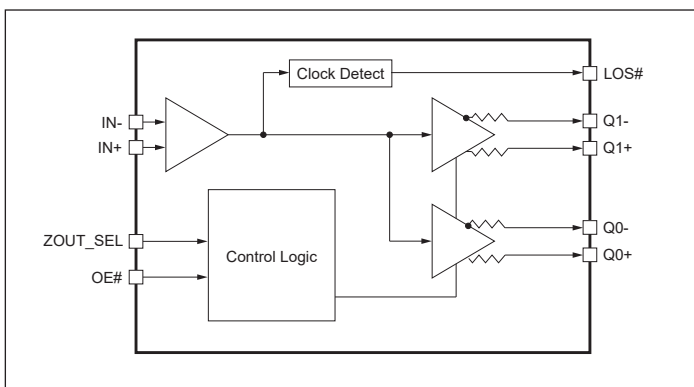


2-Output Low-Power Fanout Clock Buffer for PCIe 6.0/7.0 Application

Description

The PI6CB332002 is a low-power PCIe® 5.0/6.0 and PCIe 7.0 compatible clock buffer. It takes a reference input to fanout 2 low-power differential HCSL outputs up to 400MHz, with on-chip terminations for 85Ω or 100Ω output impedance. An individual OE pin for each output provides easier power management. The device also supports Power Down Tolerant (PDT), automatic output clock parking upon loss of input clock, and Flexible Startup Sequencing features.

Block Diagram



Features

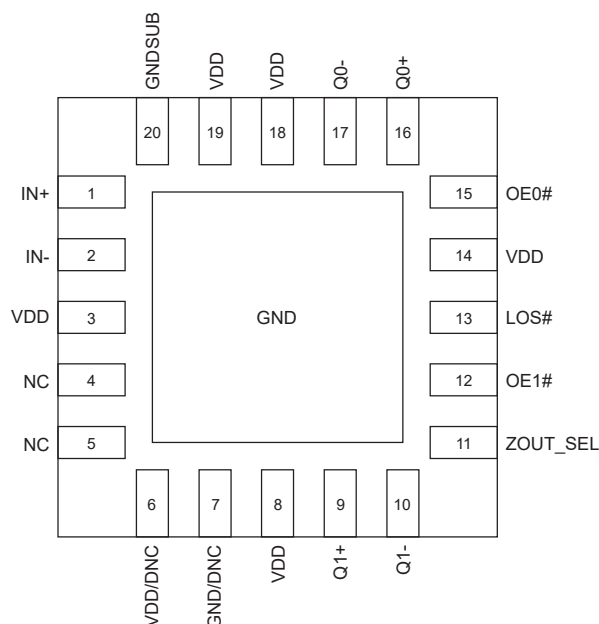
- 2 Low-Power HCSL Outputs with On-Chip Termination
- 85Ω or 100Ω Pin Selectable Output Impedance
- Individual Output Enable
- Supports I/O Power Down Tolerant
- Flexible Power Supply Startup Sequencing
- Automatic Output Clock Parking Upon Loss of Input Clock
- Differential Output-to-Output Skew <50ps
- Additive Phase Jitter
 - PCIe 5.0: Typical 5fs RMS
 - PCIe 6.0: Typical 3fs RMS
 - DB2000QL: Typical 10fs RMS
- 3.3V Supply Voltage
- Temperature Range: -40°C to 105°C
- Packaging (Pb-free & Green):
 - 20-pin, 3mm x 3mm, TQFN (W-QFN3030-20) (ZNA)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.

<https://www.diodes.com/quality/product-definitions/>

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin Number	Pin Name	Type		Description
1	IN+	Input	Diff.	True clock input. PDT. Internal pull down.
2	IN-	Input	Diff.	Complementary clock input. Internal pull up.
3	VDD	Power		Power supply.
4	NC			No connect.
5	NC			No connect.
6	VDD/DNC	Power/DNC		Power supply or floating.
7	GND/DNC	GND/NC		Ground or no connect.
8	VDD	Power		Power supply.
9	Q1+	Output	Diff.	True clock output.
10	Q1-	Output	Diff.	Complementary clock output.
11	ZOUT_SEL	Input	CMOS	Input to select differential output impedance 0 = 85Ω, 1 = 100Ω internal pull down, PDT.
12	OE1#	Input	CMOS	Active low input for enabling output 1. 0 = Enable output. 1 = Disable output. Internal pull up. PDT.
13	LOS#	Output	Open Drain	Open drain output, needs external pull up, Low output indicates loss of input clock signal, PDT.
14	VDD	Power		Power supply.

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Pin Number	Pin Name	Type		Description
15	OE0#	Input	CMOS	Active low input for enabling output 0. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
16	Q0+	Output	Diff.	True clock output.
17	Q0-	Output	Diff.	Complementary clock output.
18	VDD	Power		Power supply.
19	VDD	Power		Power supply.
20	GNDSUB	GND		Ground for substrate.
EPAD	GND	Power		Connect epad to ground.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Supply Voltage to Ground Potential, V_{DDXX}	-0.5V to +3.9V
Input Voltage	-0.5V to $V_{DD} + 0.3V$, not exceed 3.9V
Input Voltage (PDT Pin)	-0.5V to +3.9V
ESD Protection (HBM)	2000V
I_{out} (Output Current Continuous)	30mA
I_{out} (Output Current Surge).....	60mA
Junction Temperature	150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current	All outputs active @100MHz		35	45	mA
$I_{DD\_CLKOUT\_PD}$	Power Supply Current when Outputs are Disabled	All outputs are low/low		18	25	mA
$I_{DD\_CLKIN\_PD}$	Power Supply Current for Clock Input Disable	Clock IN+/- OFF		15	22	mA
T_A	Ambient Temperature	Industrial grade	-40		105	°C

Note:

1. Outputs drive 10 inch trace.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal Pull up Resistance			120		K Ω
R_{dn}	Internal Pull down Resistance			120		K Ω
L_{PIN}	Pin Inductance				7	nH

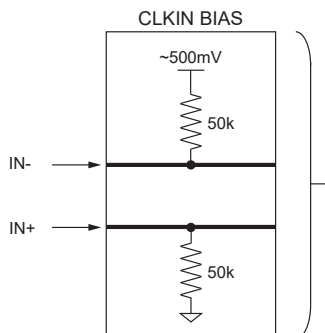


Figure 1. Input Clock Bias Network

LVCMOS DC Electrical Characteristics

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs	$0.75 \times V_{DD}$		$0.3 + V_{DD}$	V
V_{IL}	Input Low Voltage	Single-ended inputs	-0.3		$0.25 \times V_{DD}$	V
I_{IH}	Input High Current	Single-ended inputs with pull-down resistor, $V_{IN} = V_{DD}$			50	uA
		Differential inputs IN+/-, $V_{IN} = V_{DD}$			100	
I_{IL}	Input Low Current	Single-ended inputs with pullup resistor, $V_{IN} = 0$	-50			μA
		Differential inputs IN+/-, $V_{IN} = 0$	-100			
C_{IN}	Input Capacitance		1.5		5	pF

HCSL Input Characteristics⁽¹⁾

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	$V_{DD} = 3.3V$	20	100	400	MHz
V_{IHDIF}	Diff. Input High Voltage ⁽³⁾	IN+, IN-, single-end measurement	330		1150	mV
V_{ILDIF}	Diff. Input Low Voltage ⁽³⁾	IN+, IN-, single-end measurement	-300	0	300	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value ($V_{IHDIF} - V_{ILDIF}$)	200			mV
V_{COM}	Common mode voltage		100		1200	mV
t_{RF}	Diff. Input Slew Rate ⁽²⁾		0.7			V/ns
I_{IN}	Diff. Input Leakage Current	$V_{IN+} = V_{DD}$, $V_{IN-} = 0$	-40		100	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45		55	%
t_{jc-c}	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

Note:

- Guaranteed by design and characterization, not 100% tested in production
- Slew rate measured through +/-75mV window centered around differential zero
- The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is $(V_{IH} - V_{IL})/2$

HCSL Output Characteristics

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output voltage high		660	780	900	mV
V_{OL}	Output voltage low		-150	20	150	mV

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Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V _{cross absolute}	Absolute Crossing point Voltage		250		550	mV
V _{cross_var}	Crossing point voltage variation				140	mV
f _{OUT}	Output Frequency			100	400	MHz
t _{RF}	Rise time and fall time ^(1,2,3)	Scope averaging on, 10 inch trace	1.5		4	V/ns
Dt _{RF}	Slew rate matching ^(1,2,4)	Scope averaging on, 10 inch trace			20	%
t _{SKEW}	Output Skew ^(1,2)	Averaging on, V _T = 50%			50	ps
t _{DC}	Diff. Output Duty Cycle	Measured differentially	45		55	%
T _{pd}	Propagation Delay			2.0	3	ns
t _{OElat}	Output Enable Latency	Q start after OE# assertion Q stop after OE# deassertion	4	5	10	clocks
t _{LOSAassert}	LOS Assert Time	Time from disappearance of input clock to LOS assert		200	300	ns
t _{LOSDeassert}	LOS De-assert Time	Time from appearance of input clock to LOS de-assert		6	9	clocks

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the V_{swing} voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured through +/-75mV window centered around differential zero
5. Duty cycle distortion is the difference in duty cycle between the out and input clock

HCSL Output AC Characteristics - Phase Jitter

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Typ.	Max.	Specification Limit	Units
t _{jphPCIeG1-CC}	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC ≤ -0.5%	PCIe Gen 1 (2.5 GT/s)	1300		86,000	fs p-p
t _{jphPCIeG2-CC}		PCIe Gen 2 Hi Band (5.0 GT/s)	58		3,100	fs RMS
t _{jphPCIeG3-CC}		PCIe Gen 2 Lo Band (5.0 GT/s)	4		3,000	
t _{jphPCIeG4-CC}		PCIe Gen 3 (8.0 GT/s)	19		1,000	
t _{jphPCIeG5-CC}		PCIe Gen 4 (16.0 GT/s)	19		500	
t _{jphPCIeG6-CC}		PCIe Gen 5 (32.0 GT/s)	5	12.8	150	
t _{jphPCIeG6-CC}		PCIe Gen 6 (64.0 GT/s)	3	7.7	100	
t _{jphPCIeG1-IR}	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC ≤ -0.3%	PCIe Gen 1 (2.5 GT/s)	111			fs RMS
t _{jphPCIeG2-IR}		PCIe Gen 2 (5.0 GT/s)	51			
t _{jphPCIeG3-IR}		PCIe Gen 3 (8.0 GT/s)	23			
t _{jphPCIeG4-IR}		PCIe Gen 4 (16.0 GT/s)	22			
t _{jphPCIeG5-IR}		PCIe Gen 5 (32.0 GT/s)	6	9.5		
t _{jphPCIeG6-IR}		PCIe Gen 6 (64.0 GT/s)	4	7.1		

Note: The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 6.0, Revision 1.0. For the exact measurements

Applications Information

Power Down Tolerant Pins

Pins that are Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the PI6CB332002 may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the PI6CB332002 before it has received power.

Flexible Startup Sequencing

PI6CB332002 devices support Flexible Startup Sequencing (FSS), IN+/- pins are PDT. FSS allows application of CLKIN at different times in the device/system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table shows the supported sequences; that is, the PI6CB332002 devices can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

Loss of Signal and Automatic Clock Parking

The PI6CB332002 buffer has a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOS# pin (the “#” suffix indicates “bar”, or active-low). Figure 2 shows the LOS# de-assertion timing.

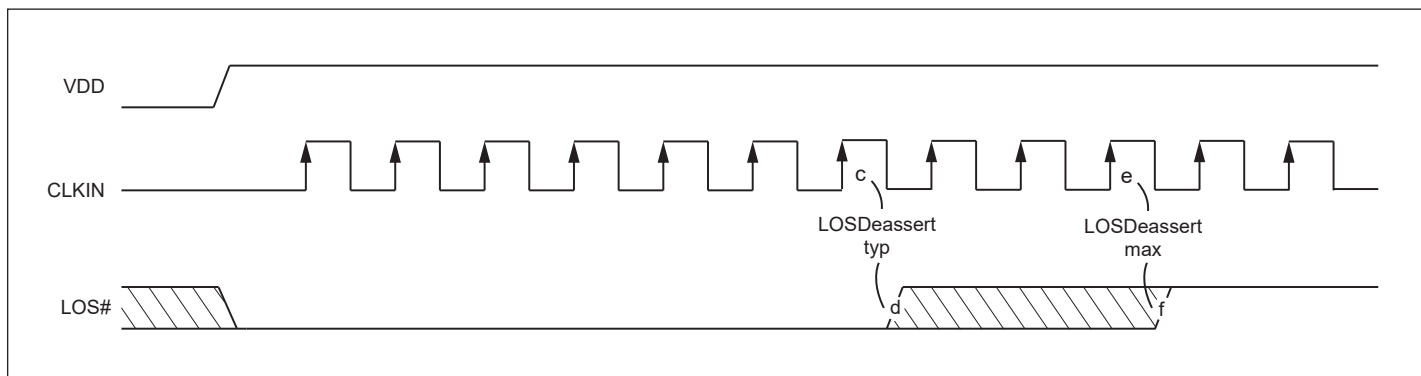


Figure 2. LOS# De-assert Timing

The following diagram shows the LOS# assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the inputs to a Low/Low state after an LOS event. For exact timing, see Electrical Characteristics.

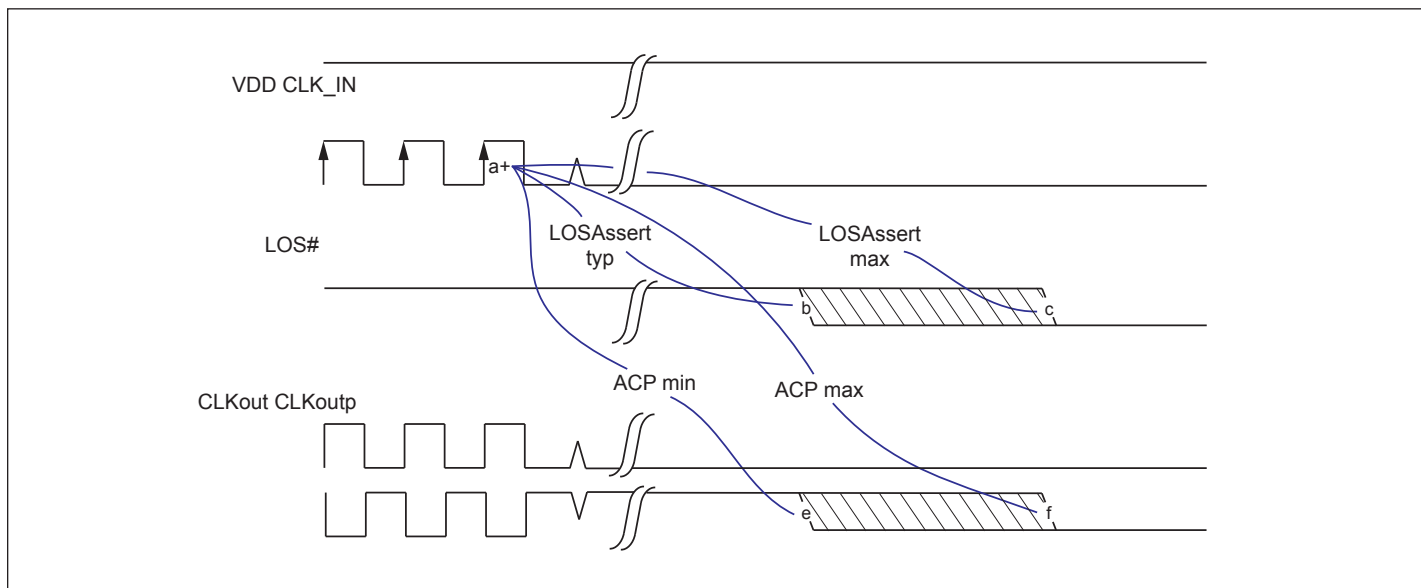


Figure 3. LOS# Assert Timing

Test Load

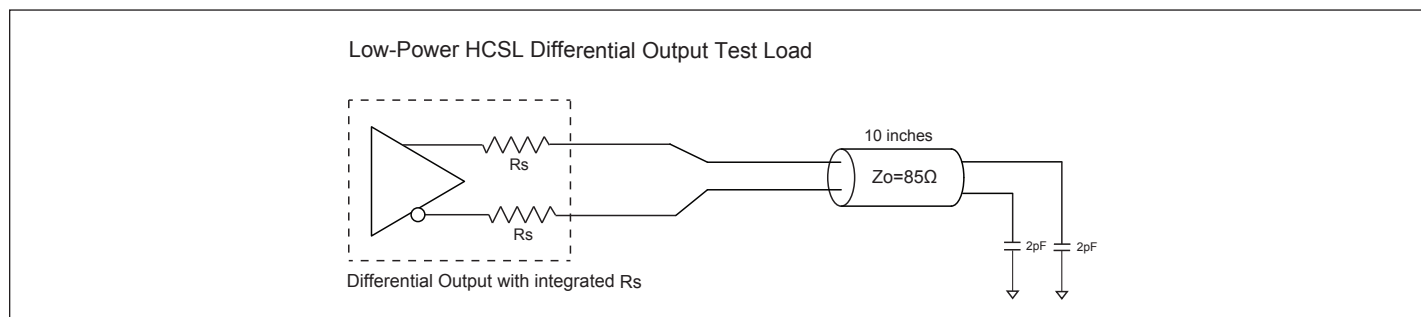


Figure 4. Low Power HCSL Test Circuit

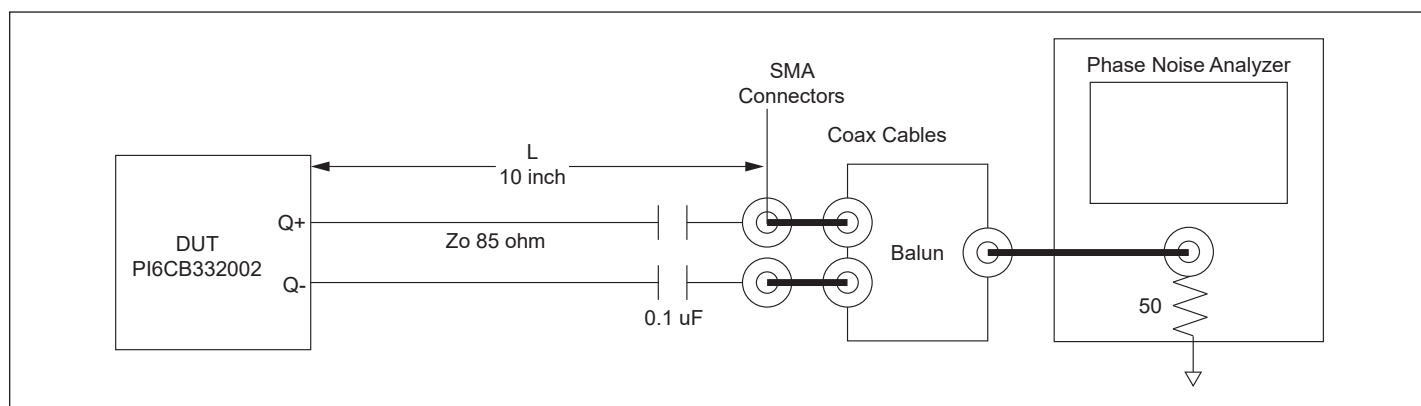


Figure 5. Test Set Up for Phase Jitter Measurement

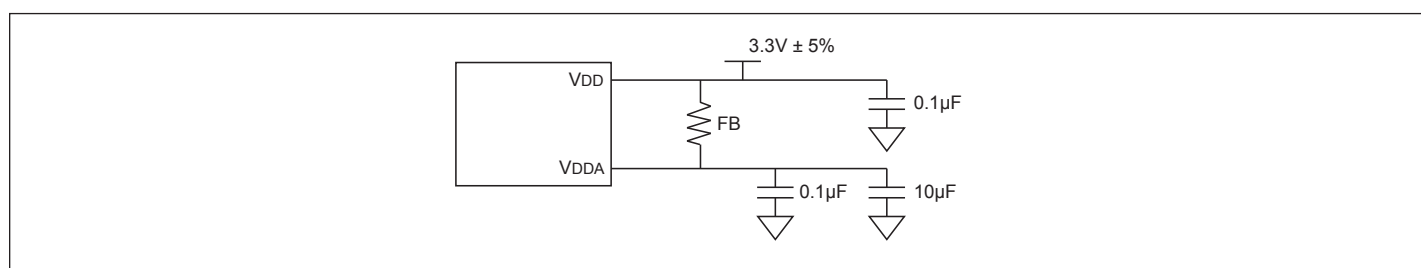


Figure 6. Power Supply Filter

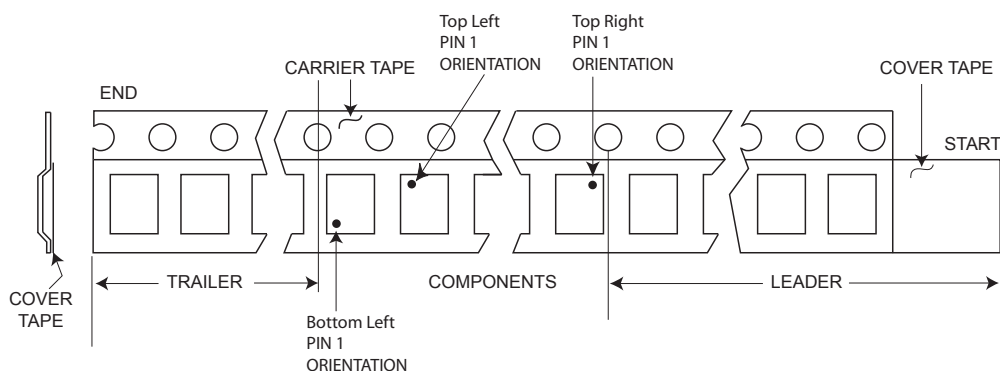
PI6CB332002

Part Marking

CB3320
02ZNAE
YWXX

Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code

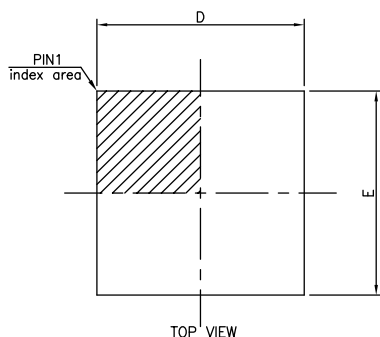
Package Information



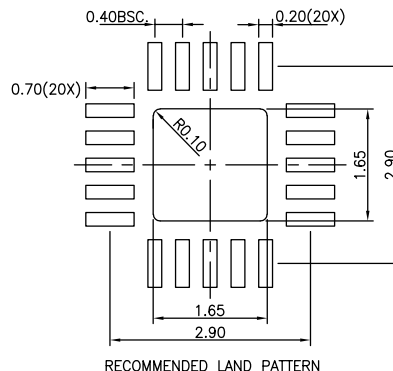
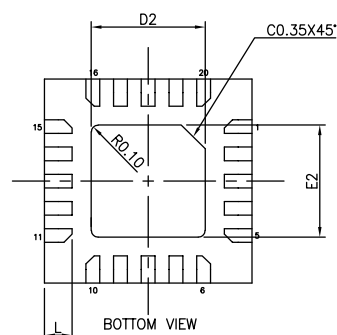
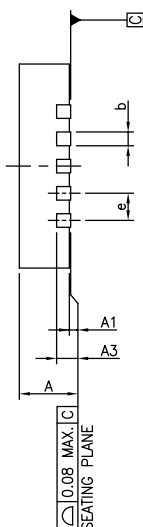
PI6CB332002

Packaging Mechanical

20-TQFN (W-QFN3030-20) (ZNA)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
L	0.30	0.40	0.50
e	0.40 BSC		



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. REFER JEDEC MO-220
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.


DATE: 09/25/23
DESCRIPTION: 20 - Contact, TQFN (W-QFN3030-20)
PACKAGE CODE: ZNA (ZNA20)
DOCUMENT CONTROL #: PD-2169
REVISION: B

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Sn Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.02 grams (Approximate)

Ordering Information

Orderable Part Number	Package Code	Package Description	Pin 1 Orientation	Temperature
PI6CB332002ZNAEX	ZNA	20-Contact, TQFN (W-QFN3030-20)	Top Right Corner	-40~105°C
PI6CB332002ZNAEX-13R	ZNA	20-Contact, TQFN (W-QFN3030-20)	Top Left Corner	-40~105°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. A = For 85Ω or 100Ω output impedance
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: <https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf>

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