ACS71010

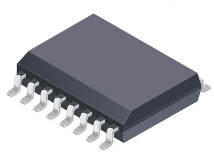
High Accuracy, Hall-Effect Current Sensor with Adjustable FAULT Output and Reference Voltage in SOICW-16 Package

FEATURES AND BENEFITS

- High operating bandwidth for fast control loops or where high-speed currents are monitored
  - □ 400 kHz bandwidth
  - □ 1.1 µs typical response time
- High performance for optimized energy applications
  - □ <±0.6% sensitivity error and ±4 mV maximum offset voltage over temperature (3σ, –40°C to 105°C)
  - □ Non-ratiometric operation with V_{REF} output
  - □ Differential sensing for high immunity to external magnetic fields
  - □ No magnetic hysteresis
- Adjustable fast overcurrent fault with 1 µs typical response time
- Low internal primary conductor resistance 0.85 mΩ
- UL 62368-1 (edition 3) certification, highly isolated compact SOICW-16 surface mount package
  - □ 5000 V_{RMS} withstand voltage
  - □ 1097 V_{RMS} / 1550 V_{DC} basic insulation voltages
  - □ 565 V_{RMS} / 800 V_{DC} reinforced insulation voltages
- Optimized temperature range, –40°C to 105°C, with functional operation up to 125°C
- Grade 2 AEC-Q100, automotive qualified (pending)

PACKAGE: 16-Pin SOICW (suffix MA)

Not to scale



DESCRIPTION

The ACS71010 is a fully integrated Hall-effect current sensor in a SOICW-16 package that is factory-trimmed to provide high accuracy over the entire operating range without the need for customer programming. The current is sensed differentially by two Hall plates that subtract out interfering external common-mode magnetic fields.

The package construction provides high isolation by magnetically coupling the field generated by the current in the conductor to the monolithic Hall sensor IC which has no physical connection to the integrated current conductor. The MA package is optimized for higher isolation with a withstand voltage, 5000 V_{RMS}, and 0.85 mΩ conductor resistance.

The ACS71010 has functional features that are externally configurable and robust without the need for programming. A fast overcurrent fault output provides short-circuit detection for system protection with a fault threshold that is proportional to the current range and can be set with an analog input. The reference pin provides a stable voltage that corresponds to the 0 A output voltage. This reference voltage allows for differential measurements as well as a device-referred voltage to set the overcurrent fault threshold.

Devices are RoHS compliant and lead (Pb) free with 100% matte-tin-platted leadframes.

APPLICATIONS

- Solar (PV) Inverters
  - □ PV Monitoring
  - □ MPPT
- EV Charging
- Energy Storage Systems (ESS)
- Power Supplies (UPS, SMPS)
- DC/AC Phase Current Sensing

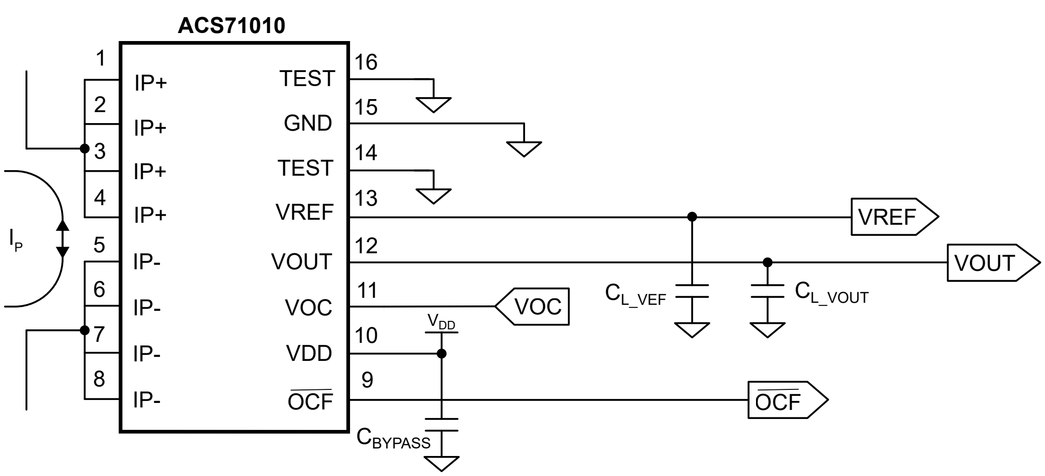


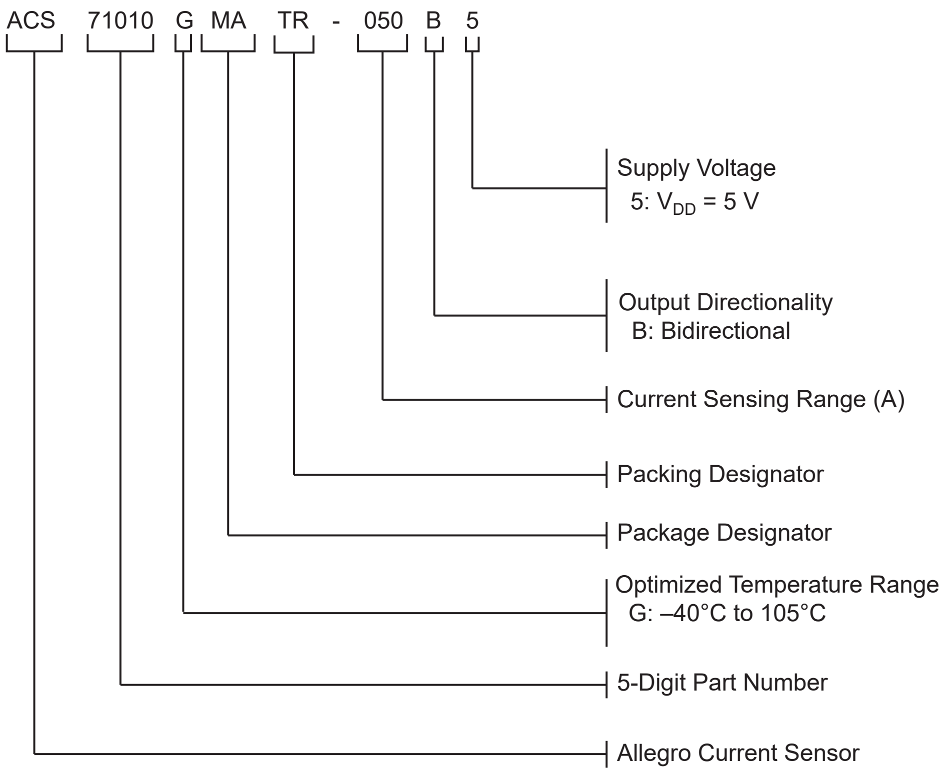
Figure 1: Typical Bidirectional Application
(refer to "Application and Theory" on page 16 for additional application circuits)

The device outputs an analog signal, V_{OUT}, that varies linearly with the AC or DC primary current, I_P, within the ranges specified.

SELECTION GUIDE

Part Number	Current Sensing Range (A)	Sensitivity (mV/A)	Supply Voltage V_{DD} (V)	Quiescent Voltage Output V_{QVO} (V)	Optimized Temperature Range T_A (°C)	Packing
ACS71010GMATR-050B5	±50	40	5	2.5	–40 to 105	1000 pieces per 13-inch reel
ACS71010GMATR-080B5	±80	25				

PART NAMING SPECIFICATION



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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Min.	Max.	Unit
Supply Voltage	V_{DD}		–0.5	6.5	V
Output Voltage	V_O	Applies to VOUT, VREF, and $\overline{\text{OCF}}$	–0.5	(V_{DD} + 0.7) < 6.5	V
Input Voltage	V_I	Applies to TEST and VOC	–0.5	(V_{DD} + 0.7) < 6.5	V
Operating Ambient Temperature	T_A		–40	150	°C
Storage Temperature	T_{STG}		–65	165	°C
Maximum Junction Temperature	$T_{J(MAX)}$	Sensing range of sensor is limited by $T_{J(MAX)}$ = 165°C	–	165	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Withstand Voltage [1][2]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	5000	V_{RMS}
Working Voltage for Basic Insulation [2]	V_{WVBI}	Maximum approved working voltage for basic insulation according to UL 62368-1 (edition 3)	1550	V_{PK} or V_{DC}
			1097	V_{RMS}
Working Voltage for Reinforced insulation [2]	V_{WVRI}	Maximum approved working voltage for reinforced insulation according to UL 62368-1 (edition 3)	800	V_{PK} or V_{DC}
			565	V_{RMS}
Surge Voltage	V_{SURGE}	1.2/50 µs waveform, tested in dielectric fluid to determine the intrinsic surge immunity of the isolation barrier	10000	V_{PK}
Impulse Withstand Voltage	$V_{IMPULSE}$	1.2/50 µs waveform, tested in air	7071	V_{PK}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	8	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	8	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	105	µm
Comparative Track Index	CTI	Material Group II	400 to 599	V

[1] Production tested for 1 second per UL 62368-1 (edition 3).
[2] Certification pending.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the standard MA/LA Current Sensor Evaluation Board (ACSEVB-MA16-LA16)	20	°C/W
Package Thermal Metric (Junction to Top)	Ψ_{JT}		2.4	°C/W
Package Thermal Resistance (Junction to Case)	$R_{\theta JC}$	Simulated per the methods in JESD51-1	13.7	°C/W
Package Thermal Resistance (Junction to Board)	$R_{\theta JB}$	Simulated per the methods in JESD51-8	13.5	°C/W

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	0.85	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	4.2	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	3	–	–

PINOUT DIAGRAM AND TERMINAL LIST TABLE

Terminal List Table

Number	Name	Description
1, 2, 3, 4	IP+	Positive terminal for current being sensed
5, 6, 7, 8	IP–	Negative terminal for current being sensed
9	$\overline{\text{OCF}}$	Overcurrent fault output, active low
10	VDD	Device power supply terminal
11	VOC	Overcurrent fault operation point analog input; if VOC pin is not used, GND for optimal ESD performance
12	VOUT	Analog output signal
13	VREF	Zero-current voltage reference
14	TEST	No connect, connect to GND for optimal ESD performance
15	GND	Device ground terminal
16	TEST	No connect, connect to GND for optimal ESD performance

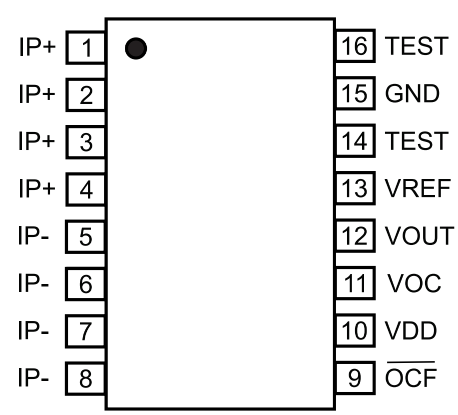

Figure 2: MA Pinout Diagram

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FUNCTIONAL BLOCK DIAGRAM

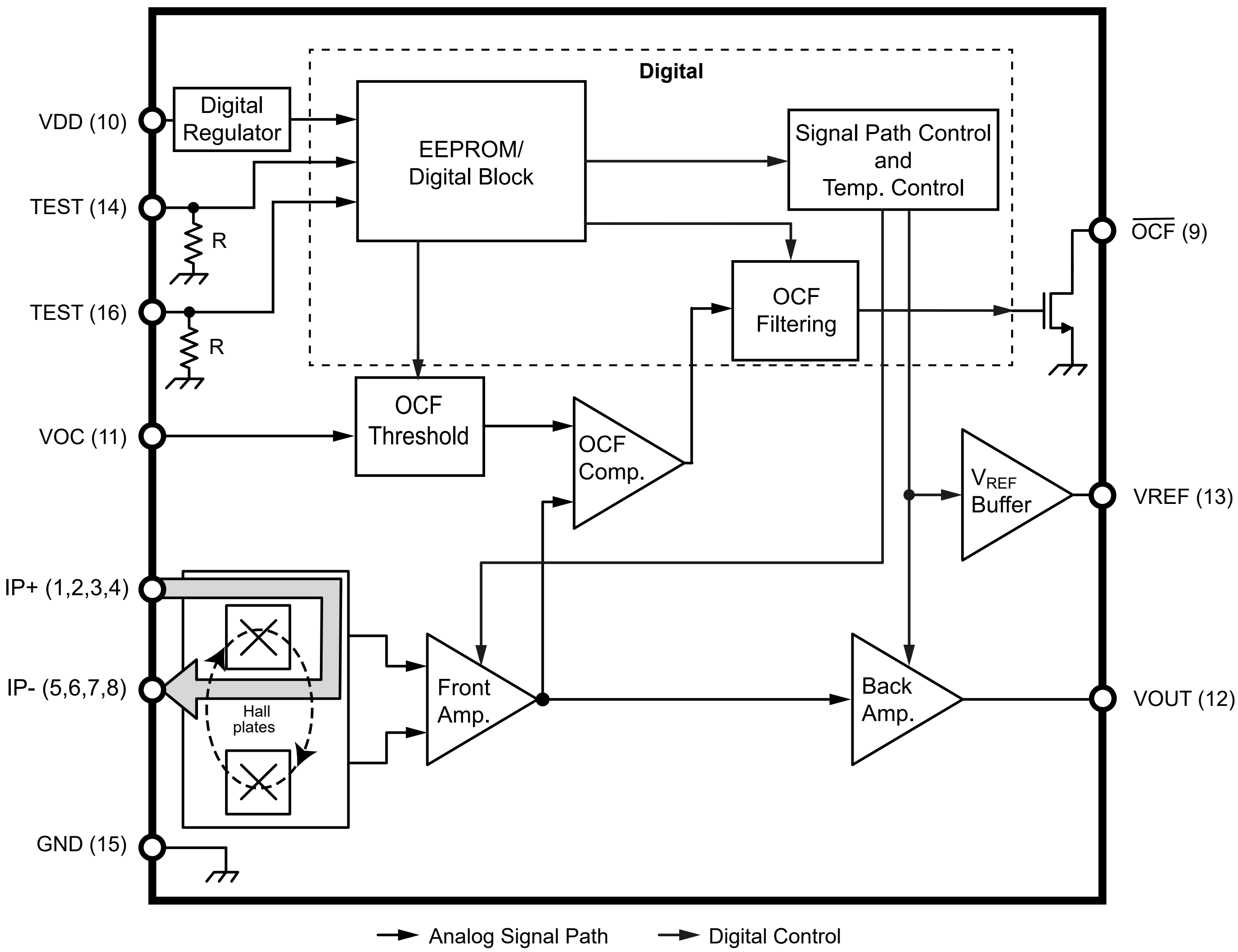

Figure 3: Functional Block Diagram

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	5 V variant	4.75	5	5.25	V
Supply Current	I_{CC}	5 V variant, no load on VOUT, $\overline{\text{OCF}}$, and VOC	–	13	18	mA
Supply Bypass Capacitor	C_{BYPASS}		0.1	–	–	µF
Output Resistive Load [1]	R_{L_VOUT}		10	–	–	kΩ
Output Capacitive Load [1]	C_{L_VOUT}		–	1	6	nF
Power-On Reset Voltage	V_{POR_H}	T_A = 25°C, V_{DD} rising 1 V/ms	2.6	2.9	3.1	V
	V_{POR_L}	T_A = 25°C, V_{DD} falling 1 V/ms	2.2	2.5	2.8	V
Power-On Hysteresis	V_{POR_HYS}		250	–	–	mV
Power-On Time	t_{PO}		100	–	–	µs
Overvoltage Detection (OVD) Threshold	V_{OVD_H}	T_A = 25°C, V_{DD} rising 1 V/ms	6.1	6.3	6.8	V
	V_{OVD_L}	T_A = 25°C, V_{DD} falling 1 V/ms	5.6	5.8	6.1	V
Overvoltage Detection Hysteresis	V_{OVD_HYS}		–	660	–	mV
OVD Delay Time	t_{OVD_E}		60	90	120	µs
	t_{OVD_D}		–	7	–	µs
OUTPUT SIGNAL CHARACTERISTICS (VOUT)						
Saturation Voltage [2]	V_{SAT_H}	R_{L_VOUT} = 10 kΩ to GND	V_{DD} – 0.1	–	–	V
	V_{SAT_L}	R_{L_VOUT} = 10 kΩ to GND	–	–	0.1	V
Short Circuit Current	I_{SC_VOUT}	VOUT to GND	–	25	–	mA
Bandwidth	BW	Small signal –3 dB, C_{L_VOUT} = 6 nF	–	400	–	kHz
Rise Time	t_R	T_A = 25°C, C_{L_VOUT} = 6 nF	–	0.7	2.5	µs
Response Time	t_{RESP}	T_A = 25°C, C_{L_VOUT} = 6 nF	–	1.1	2.5	µs
Propagation Delay	t_{PD}	T_A = 25°C, C_{L_VOUT} = 6 nF	–	0.7	2	µs
Noise Density	N_D	5 V variant, T_A = 25°C, C_{L_VOUT} = 6 nF	–	350	–	µA/√Hz
Noise	N	5 V variant, T_A = 25°C, C_{L_VOUT} = 6 nF	–	277	–	mA_{RMS}
Common-Mode Field Rejection	CMFR	Input-referred error due to common-mode field	–	4	–	mA/G
VOUT Output Resistance	R_O		–	7.3	–	Ω

[1] Validated by design and characterization.
[2] The sensor may continue to respond to current beyond the specified Current Sensing Range, I_{PR}, until the output saturates at the high or low saturation voltage; however, the linearity and performance beyond the specified Current Sensing Range are not validated.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
REFERENCE OUTPUT CHARACTERISTICS (VREF)						
Reference Resistive Load	R_{L_VREF}		10	–	–	kΩ
Reference Capacitive Load	C_{L_VREF}		–	–	6	nF
Reference Source/Sink Current Limit	I_{REF}	Maximum current V_{REF} can passively source	–	25	–	mA
Reference Slew Rate	SR_{REF}	C_{L_REF} = 0 nF, R_{L_VREF} = 0 Ω	0.8	–	–	V/µs
OVERCURRENT FAULT CHARACTERISTICS ($\overline{OCF}$)						
Overcurrent FAULT Pull-Up Resistor	R_{L_FAULT}		4.7	–	500	kΩ
Overcurrent FAULT Output Error	E_{OC}	T_A = 25°C	–10	–	10	$\%I_{OCR}$ [1]
Overcurrent FAULT Output Low Voltage	V_{FAULT_L}	R_{L_FAULT} = 10 kΩ, fault condition present	–	0.07	0.4	V
Overcurrent FAULT Leakage Current	I_{FAULT_OFF}	R_{L_FAULT} = 10 kΩ, no fault condition present	–	100	–	nA
Overcurrent FAULT Hysteresis	I_{OC_HYS}	5 V variant	–	6	–	%FS
Overcurrent FAULT Response Time [1]	t_{OC_RESP}		–	1	1.5	µs
VOC Input Linear Operating Range	V_{OR_VOC}	5 V variant, T_A = 25°C	0.5	1	2	V

[1] Validated by design and characterization.
[2] Where I_{OCR} is the specific point at which the $\overline{OCF}$ trigger occurs and is set by V_{OC} voltage within V_{OR_VOC}.

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			Minimum			Maximum		
Characteristic	**Symbol**	**Test Conditions**	**–6σ [1]**	**–3σ**	**Typ.**	**3σ**	**6σ [1]**	**Units**
NOMINAL PERFORMANCE								
Current Sensing Range [2]	I_{PR}	Limited by $T_{J(MAX)}$ = 165°C	–50		–	50		A
Sensitivity	Sens	$I_{PR(MIN)} < I_P < I_{PR(MAX)}$	–		40	–		mV/A
Overcurrent Fault Operating Range	I_{OCF_OR}		50		–	200		%FS
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–		2.5	–		V
TOTAL ERROR [$V_{IOUT(ACTUAL)}$ – ($Sens_{(IDEAL)}$ × I_{PR} + V_{REF})]/($Sens_{(IDEAL)}$ × I_{PR}) × 100 AND TOTAL ERROR COMPONENTS								
Sensitivity Error (Including Linearity)	E_{SENS}	$I_P = I_{PR(MAX)}$, T_A = 25°C to 105°C	–0.95	–0.6	–	0.6	0.95	%
		$I_P = I_{PR(MAX)}$, T_A = –40°C to 25°C	–0.95	–0.55	–	0.55	0.95	%
		$I_P = I_{PR(MAX)}$, T_A = 25°C to 125°C [3]	–	–1.15	–	1.15	–	%
Reference Voltage Output Error	V_{REF_E}	I_P = 0 A, T_A = 25°C to 105°C	–3.8	–2	–	2	3.8	mV
		I_P = 0 A, T_A = –40°C to 25°C	–3.5	–2		2	3.5	mV
		I_P = 0 A, T_A = 25°C to 125°C [3]	–	–4	–	4	–	mV
Offset Error	V_{OE}	I_P = 0 A, T_A = 25°C to 105°C	–5	–3	–	3	5	mV
		I_P = 0 A, T_A = –40°C to 25°C	–4.5	–3	–	3	4.5	mV
		I_P = 0 A, T_A = 25°C to 125°C [3]	–	–4	–	4	–	mV
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C to 105°C	–6	–3.5	–	3.5	6	mV
		I_P = 0 A, T_A = –40°C to 25°C	–5.5	–3	–	3	5.5	mV
		I_P = 0 A, T_A = 25°C to 125°C [3]	–	–5.5	–	5.5	–	mV
Power Supply Offset Error	V_{OE_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–5.5	–3.3	–	3.3	5.5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–0.75	–0.5	–	0.5	0.75	%

[1] Minimum and maximum values are based on the mean ±6 sigma of the production distribution, such that 99.99% of devices lie within the interval during initial characterization.
[2] Validated by design and characterization.
[3] The ACS71010 is temperature optimized up to 105°C but functions up to 125°C based on historical data of grade 0 and grade 1 predecessors. Reaching temperatures beyond 105°C may have permanent degraded performance. Allegro only guarantees accuracy up to 105°C and 125°C values are based on characterization data.

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Characteristic	Symbol	Test Conditions	Minimum		Typ.	Maximum		Units
			–6σ [1]	–3σ		3σ	6σ [1]	
NOMINAL PERFORMANCE								
Current Sensing Range[2]	I_{PR}	Limited by T_{JMAX} = 165°C	–80		–	80		A
Sensitivity	Sens	$I_{PR(MIN)} < I_P < I_{PR(MAX)}$	–		25	–		mV/A
Overcurrent Fault Operating Range	I_{OCF_OR}		50		–	200		%FS
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–		2.5	–		V
TOTAL ERROR [$V_{IOUT(ACTUAL)}$ – ($Sens_{(IDEAL)} \times I_{PR} + V_{REF}$)]/($Sens_{(IDEAL)} \times I_{PR}$) × 100 AND TOTAL ERROR COMPONENTS								
Sensitivity Error (Including Linearity)	E_{SENS}	$I_P = I_{PR(MAX)}$, T_A = 25°C to 105°C	–0.95	–0.6	–	0.6	0.95	%
		$I_P = I_{PR(MAX)}$, T_A = –40°C to 25°C	–0.95	–0.55	–	0.55	0.95	%
		$I_P = I_{PR(MAX)}$, T_A = 25°C to 125°C [3]	–	–1.1	–	1.1	–	%
Reference Voltage Output Error	V_{REF_E}	I_P = 0 A, T_A = 25°C to 105°C	–4	–2	–	2	4	mV
		I_P = 0 A, T_A = –40°C to 25°C	–3.5	–2	–	2	3.5	mV
		I_P = 0 A, T_A = 25°C to 125°C [3]	–	–5.5	–	5.5	–	mV
Offset Error	V_{OE}	I_P = 0 A, T_A = 25°C to 105°C	–4.5	–2.5	–	2.5	4.5	mV
		I_P = 0 A, T_A = –40°C to 25°C	–4.5	–2.5	–	2.5	4.5	mV
		I_P = 0 A, T_A = 25°C to 125°C [3]	–	–4	–	4	–	mV
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C to 105°C	–6	–4	–	4	6	mV
		I_P = 0 A, T_A = –40°C to 25°C	–6	–4	–	4	6	mV
		I_P = 0 A, T_A = 25°C to 125°C [3]	–	–7.5	–	7.5	–	mV
Power Supply Offset Error	V_{OE_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–5.5	–3.3	–	3.3	5.5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–0.75	–0.5	–	0.5	0.75	%

[1] Minimum and maximum values are based on the mean ±6 sigma of the production distribution, such that 99.99% of devices lie within the interval during initial characterization.
[2] Validated by design and characterization.
[3] The ACS71010 is temperature optimized up to 105°C but functions up to 125°C based on historical data of grade 0 and grade 1 predecessors. Reaching temperatures beyond 105°C may have permanent degraded performance. Allegro only guarantees accuracy up to 105°C and 125°C values are based on characterization data.

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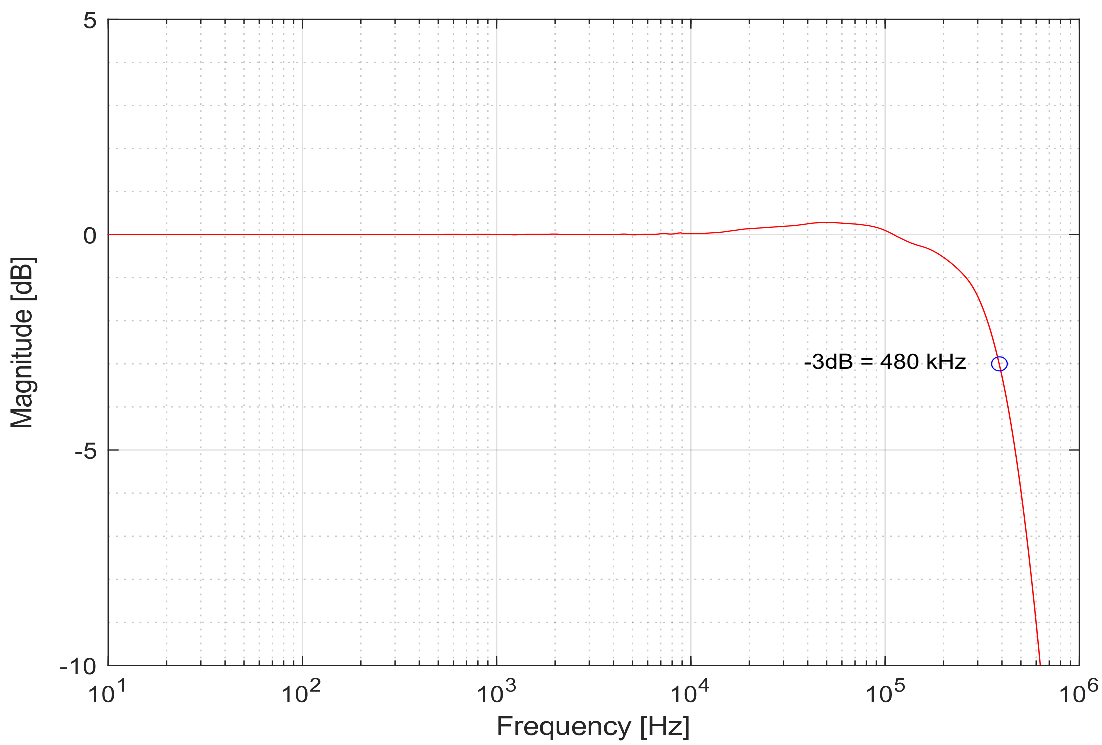
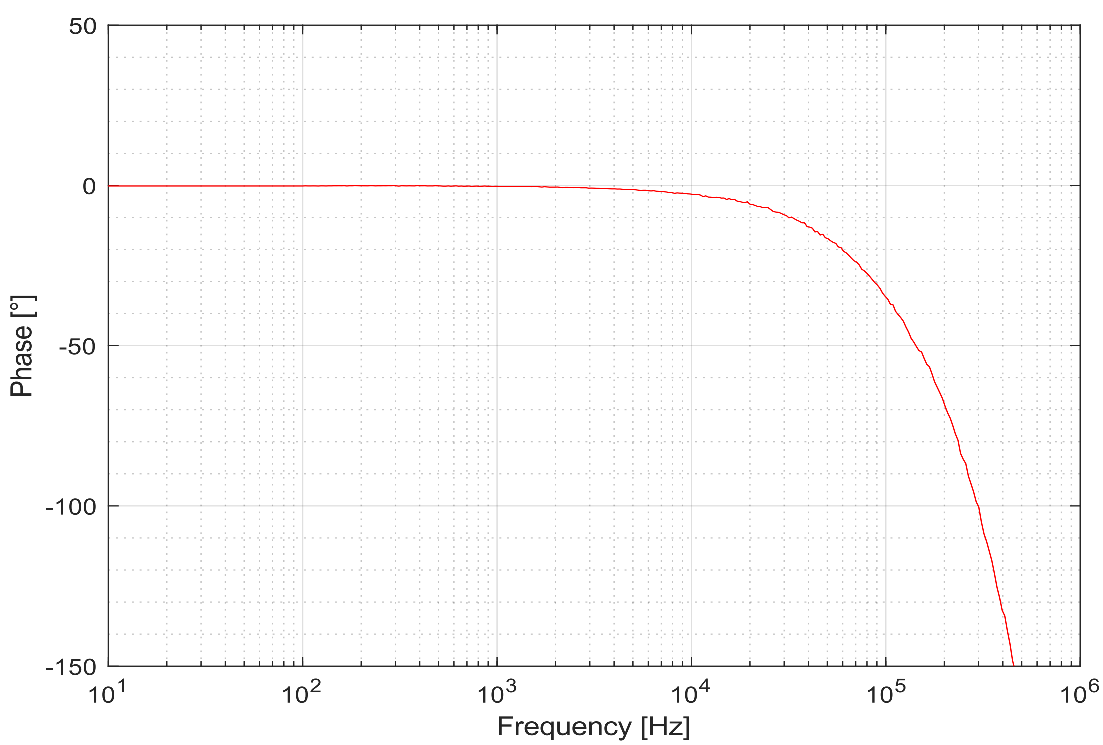
FREQUENCY RESPONSE PERFORMANCE DATA





STEP RESPONSE CHARACTERISTICS DEFINITIONS AND PERFORMANCE DATA

Response Time (t_{RESP})

The time interval between a) when the sensed input current reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value.

Propagation Delay (t_{PD})

The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

Rise Time (t_R)

The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

Response Time, Propagation Delay, Rise Time, and Output Slew Rate

Applied current step with 10%-90% rise time = 1 µs

Test Conditions: T_A = 25°C, C_{BYPASS} = 0.1 µF, C_{L_VOUT} = 6 nF

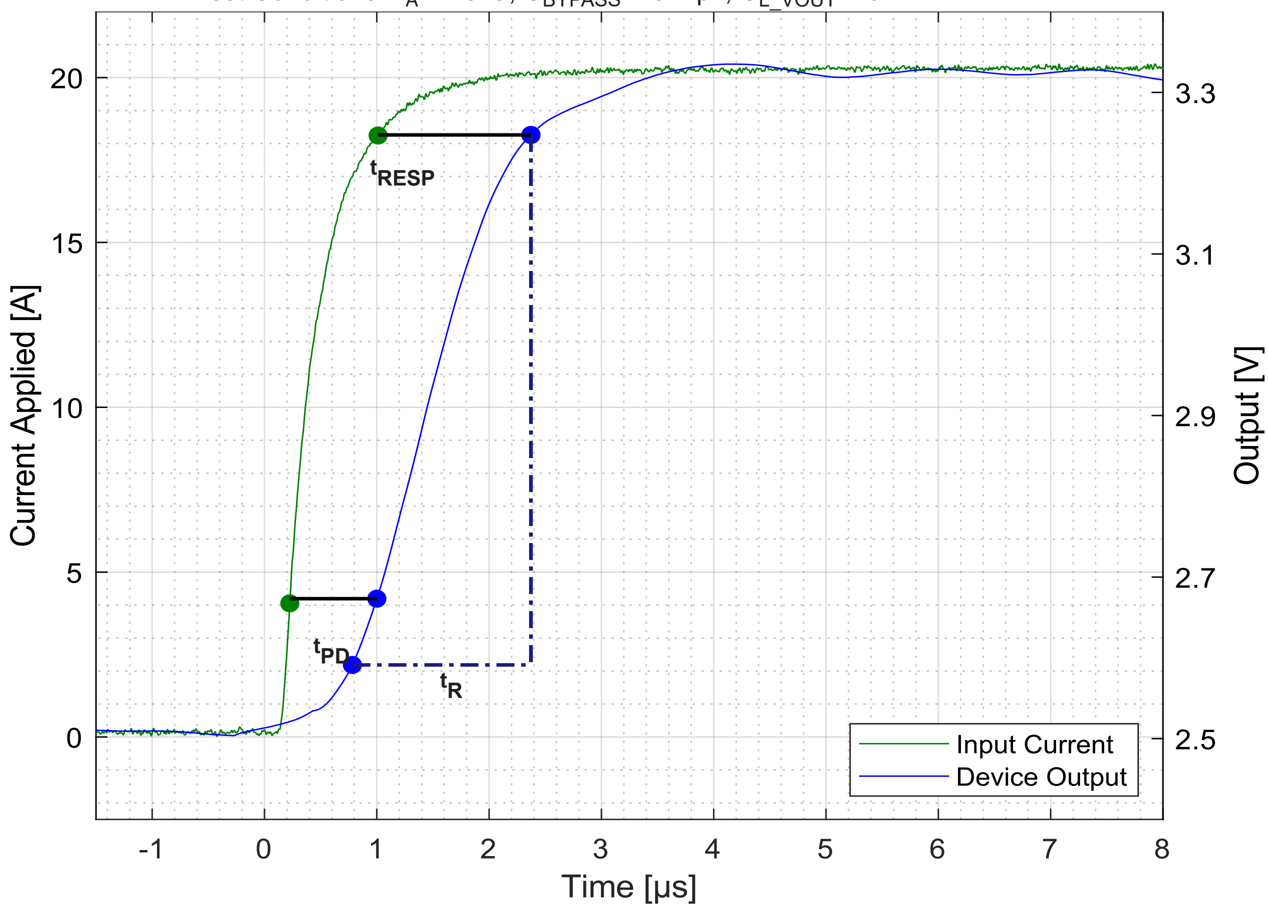


Figure 4: Step Response Performance

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DESCRIPTIONS OF POWER ON/OFF OPERATION

Introduction

To ensure that the device output is reporting accurately, the device contains an overvoltage detection flag. This internal flag on V_{OUT} can be used to alert the system when the supply voltage for the device is outside of the operational range by putting the output into a known high-impedance (high Z) state.

The graphs in this section show V_{OUT} and V_{REF} moving with V_{DD}. The voltage of V_{OUT} during a high-impedance state is most consistent with a known load (R_{L_VOUT}, C_{L_VOUT}). All figures below all use the same labeling scheme for different power thresholds. References in brackets "[ ]" are valid for Figure 5 and Figure 6.

POWER-ON OPERATION

As V_{DD} ramps up, the device V_{OUT} and V_{REF} pins are high Z until V_{DD} reaches and passes V_{POR} [1]. Once V_{DD} has passed V_{POR} [1], V_{OUT} enters normal operation.

POWER-OFF OPERATION

V_{REF} and V_{OUT} continue to report until V_{DD} is less than V_{POR} – V_{POR_HYS} [8], at which point, V_{OUT} and V_{REF} enters a high-Z state. The hysteresis on the power-on voltage prevents noise on the supply line from causing V_{OUT} to repeatedly enter and exit the high-Z state around the V_{POR} level.

NOTE: Because the device is entering a high-Z state and not driving the output, the time it takes the output to reach a steady state depends on the external circuitry used.

Voltage Thresholds

POWER-ON RESET VOLTAGE(V_{POR})

If V_{DD} falls below V_{POR} – V_{POR_HYS} [8] while in operation, the digital circuitry turns off and the output re-enters a high-Z state. After V_{DD} recovers, the output begins reporting again after the delay of t_{PO}.

OVERVOLTAGE DETECTION THRESHOLD (V_{OVD})

When V_{DD} rises above V_{OVD} [4], the output of the V_{OUT} pin goes high Z, V_{REF} be pulled to GND, and V_{OUT} is pulled to either VDD or GND, depending on the configuration (pull-up vs. pull-down) of R_{L_VOUT}.

OVERVOLTAGE DETECTION HYSTERESIS (V_{OVD_HYS})

There is hysteresis between enable and disable thresholds to reduce nuisance flagging and clears.

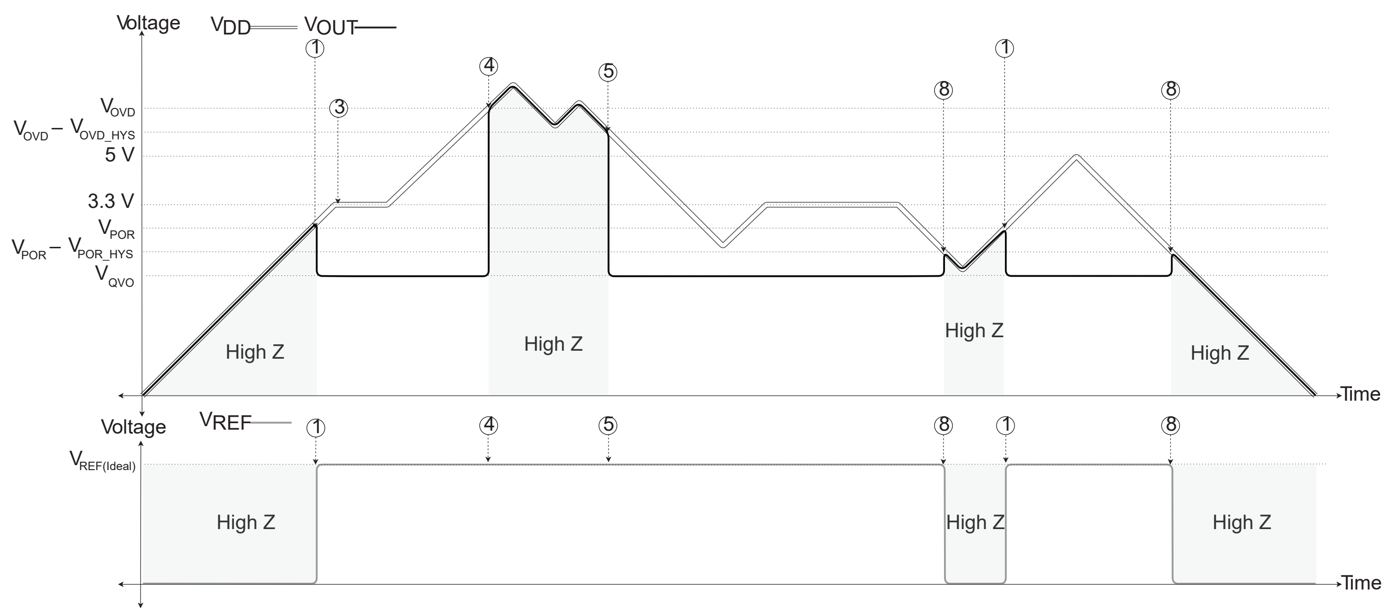

Figure 5: Power States Thresholds with V_{OUT} and V_{REF} Behavior, R_L = Pull-Up

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DESCRIPTIONS OF TIMING THRESHOLDS

POWER-ON DELAY (t_{PO})

Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, which can be seen as the time from [2] to [A] in Figure 6. After this delay, the output quickly approaches $V_{OUT(IP)}$ = Sens × I_P + V_{REF}.

OVERVOLTAGE DELAY TIME (t_{OVD_E}/t_{OVD_D})

The enable time for OVD, t_{OVD_E}, is the time from V_{OVD_H} [3] to OVD flag [B].

The disable time for OVD, t_{OVD_D}, is the time from V_{OVD} – V_{OVD_HYS} [4] to the OVD clear to normal operation [C].

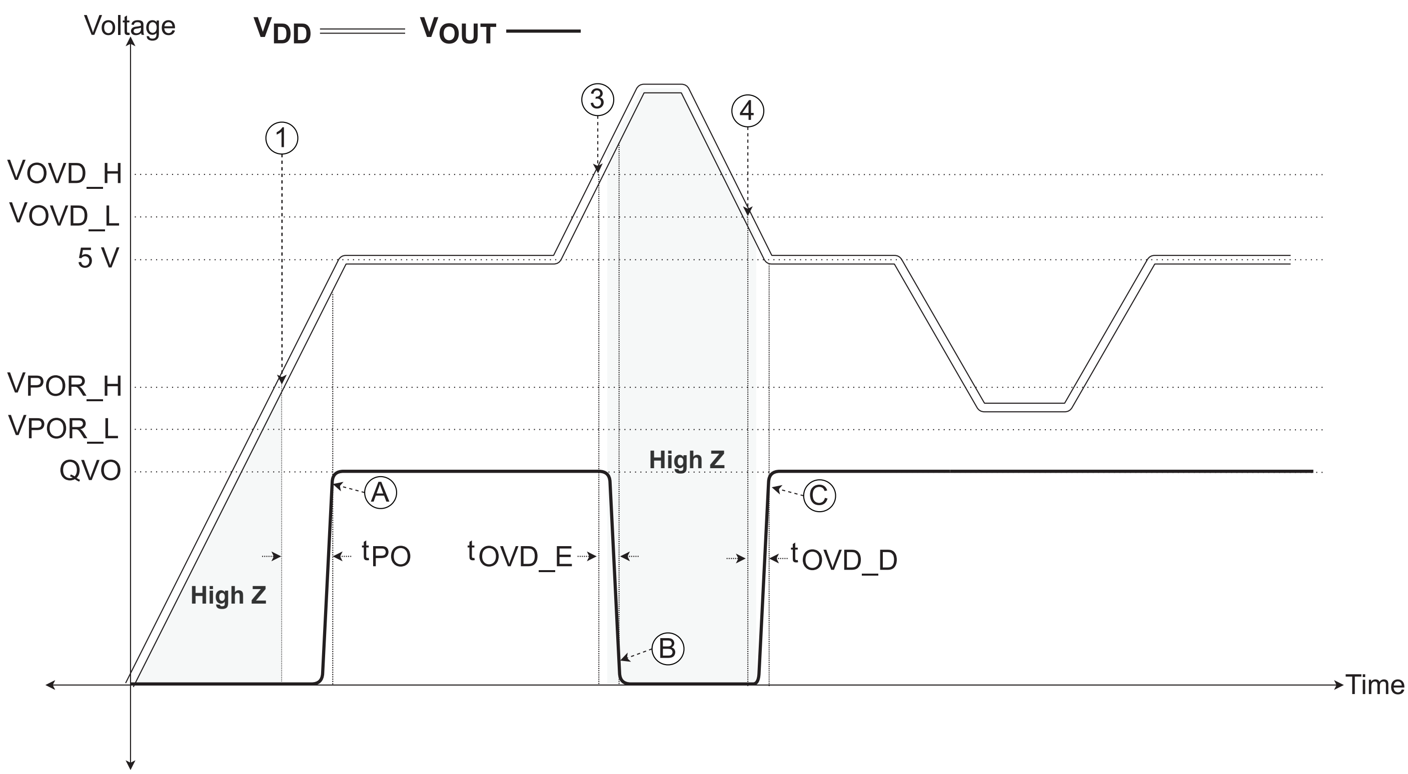

Figure 6: t_{PO} and $t_{OVD\_E/D}$ with R_L = Pull-Up

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DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Introduction

The ACS71010 is optimized over the temperature range of –40°C to 105°C. The device survives and functions at temperatures up to 125°C based on characterization data, but performance may permanently degrade and is not guaranteed.

Minimum and maximum limits included in the operating characteristics tables represent the mean ± 3 sigma (±3σ) and mean ± 6 sigma (±6σ) of the worst case mean performance observed across the specified region based on characterization. The ±3σ values given for the temperature range of 25°C to 125°C include the values given for the 25°C to 105°C range.

Quiescent Voltage Output (V_{QVO})

Quiescent Voltage Output, V_{QVO}, is defined as the voltage on the output, V_{OUT}, when no current is applied, $I_P = 0$.

$$V_{QVO} = V_{OUT\_@0A}\ [mV]$$

Quiescent Voltage Output Error (V_{QVO_E})

Quiescent Voltage Output Error, V_{QVO_E}, is defined as the deviation of V_{QVO} from the nominal target value in production testing.

$$V_{QVO\_E} = V_{QVO\_MEASURED} - V_{QVO\_IDEAL}\ [mV]$$

Power Supply Offset Error (V_{OE_PS})

Power Supply Offset Error, V_{OE_PS}, is defined as the change in V_{QVO} due to variations in the power supply voltage at a specific temperature. The Power Supply Offset Error is defined as the change in offset measured between the nominal supply voltage (V_{DD}) and V_{DD} ±E%, where E is the difference between V_{DD} and $V_{DD(MAX)}$ in percent. The error is expressed in mV to indicate how much the offset deviates from its ideal value due to changes in the supply voltage.

$$V_{OE\_PS} = V_{QVO_{@VDD}\pm E\%,T_A} - V_{QVO_{@VDD},T_A}\ [mV]$$

Sensitivity (Sens)

Sensitivity, or Sens, is defined as the ratio of the V_{OUT} swing and the current through the primary conductor, I_P. The current causes a voltage change on V_{OUT} away from V_{QVO} until V_{SAT}. The magnitude and direction of the output voltage is proportional to the magnitude and direction of the current, I_P. The proportional relationship between output voltage and current is Sensitivity, defined as:

$$Sens = \frac{V_{OUT\_IP1} - V_{OUT\_IP2}}{I_{P1} - I_{P2}}\ [mV/A]$$

where I_{P1} and I_{P2} are two different currents, and $V_{OUT}(I_{P1})$ and $V_{OUT}(I_{P2})$ are the respective output voltages, at VOUT, at those currents.

Sensitivity Error (E_{SENS})

Sensitivity Error, E_{SENS}, is the deviation of Sensitivity from the nominal sensitivity target value in production testing.

$$E_{SENS} = \frac{SENS_{MEASURED} - SENS_{IDEAL}}{SENS_{IDEAL}}\ x\ 100\ [\%]$$

Power Supply Sensitivity Error (E_{SENS_PS})

Power Supply Sensitivity Error, E_{SENS_PS}, is a measure of the change in sensitivity due to variations in the power supply voltage at a specific temperature. The Power Supply Sensitivity Error is defined as the percentage change in sensitivity measured between the nominal supply voltage (V_{DD}) and V_{DD} ±E%, where E is the difference between V_{DD} and $V_{DD(MAX)}$ in percent. The error is expressed as a percentage to indicate how much the sensitivity deviates from its ideal value due to changes in the supply voltage.

$$E_{SENS\_PS} = \frac{SEN_{@VDD\pm E\%,T_A} - SENS_{@VDD,T_A}}{SENS_{@VDD,T_A}}\ x\ 100\ [\%]$$

Output Saturation Voltage (V_{SAT_H} and V_{SAT_L})

Output Saturation Voltage, V_{SAT}, is defined as the minimum and maximum voltages the VOUT output budder can drive. V_{SAT_H} is the highest voltage the output can reach, while V_{SAT_L} is the lowest. In other states, the VOUT pin may be pulled outside of V_{SAT_L} and V_{SAT_H}. Note that changing the sensitivity does not change the V_{SAT} points.

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DEFINITIONS OF OVERCURRENT FAULT ($\overline{\text{OCF}}$) CHARACTERISTICS AND PERFORMANCE

OVERCURRENT FAULT PIN ($\overline{\text{OCF}}$)

As the output swings, if the sensed current exceeds its set threshold, the overcurrent FAULT ($\overline{\text{OCF}}$) pin triggers with an active low flag. This is internally compared with either the factory-programmed threshold or the VOC voltage. This flag trips symmetrically for the positive and negative overcurrent fault operating point.

VOLTAGE OVERCURRENT PIN (VOC)

The Voltage Overcurrent pin, or VOC, is a voltage input that is used to set the Overcurrent FAULT Threshold, I_{OCR}. There are two ways to set the threshold:1) via a resistor, R_{VOC}, between VOC and GND, or 2) by an external low-impedance voltage source connected to VOC.

The sensor has an internal factory-calibrated current source at VOC. Connecting a resistor between VOC and GND sets the voltage at VOC. I_{OCR} is set as a percentage of the full-scale sensing range of the device, $I_{PR(MAX)}$, and can be between 50% $I_{PR(MAX)}$ and 200% $I_{PR(MAX)}$.

Table 1: FAULT threshold, I_{OCR}, as set by V_{VOC}

V_{VOC} (V)		I_{OCR} (% $I_{PR(MAX)}$)
5 V variants	3.3 V variants	
Default		100
0.5	0.33	50
0.75	0.466	75
1	0.661	100
1.25	0.86	125
1.5	0.991	150
1.75	1.156	175
2	1.321	200

The voltage at VOC can also be set using an external low-impedance voltage source that overdrives the internal current supply. If the application does not require the threshold to be adjusted once the sensor is in operation, it is recommended to use a low-tolerance resistor for fixing I_{OCR}.

If the VOC pin is being driven by a non-inverted buffered V_{REF}, it is important to consider that any error from the V_{REF} pin is gained as well. For instance, if V_{REF} error is +10 mV and the gain = 4 for the non-inverting operational amplifier, then the VOC pin is 40 mV from the expected target.

OVERCURRENT FAULT OUTPUT ERROR (E_{OC})

Overcurrent FAULT Error, E_{OC}, is defined as the difference between the set current threshold and the measured current at which the $\overline{\text{OCF}}$ activates.

OVERCURRENT FAULT HYSTERESIS (I_{OC_HYS})

Overcurrent Hysteresis, or I_{OC_HYST}, is defined as the magnitude of current in percentage of the full-scale current that must drop before a fault assertion is cleared. This can be seen as the separation between the voltages [9] to [10] in Figure 7 and Figure 8.

VOC INPUT LINEAR OPERATING RANGE (V_{OR_VOC})

VOC Input Linear Operating Range, V_{OR_VOC}, is the voltage range for V_{VOC} in which the Overcurrent FAULT Threshold, I_{OCR}, varies linearly with V_{VOC}.

OVERCURRENT FAULT RESPONSE TIME (t_{OC_RESP})

Overcurrent Response Time, or t_{OC_RESP}, is defined as the time from when the input current reaches the operating point [9] until the $\overline{\text{OCF}}$ pin falls below V_{FAULT_L} [G].

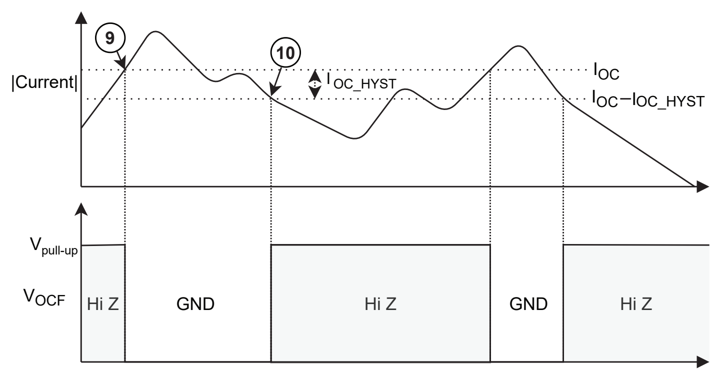

Figure 7: Fault Thresholds and $\overline{\text{OCF}}$ Pin Functionality

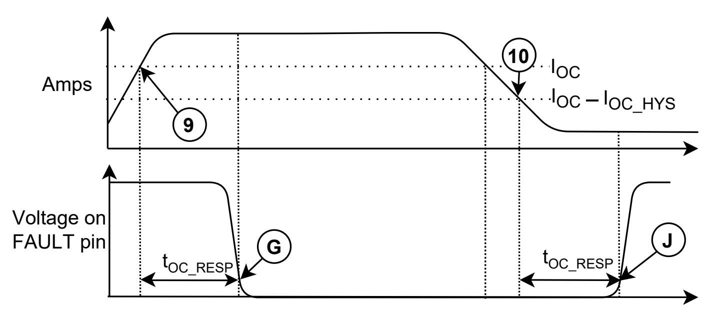

Figure 8: Fault Timing Diagram

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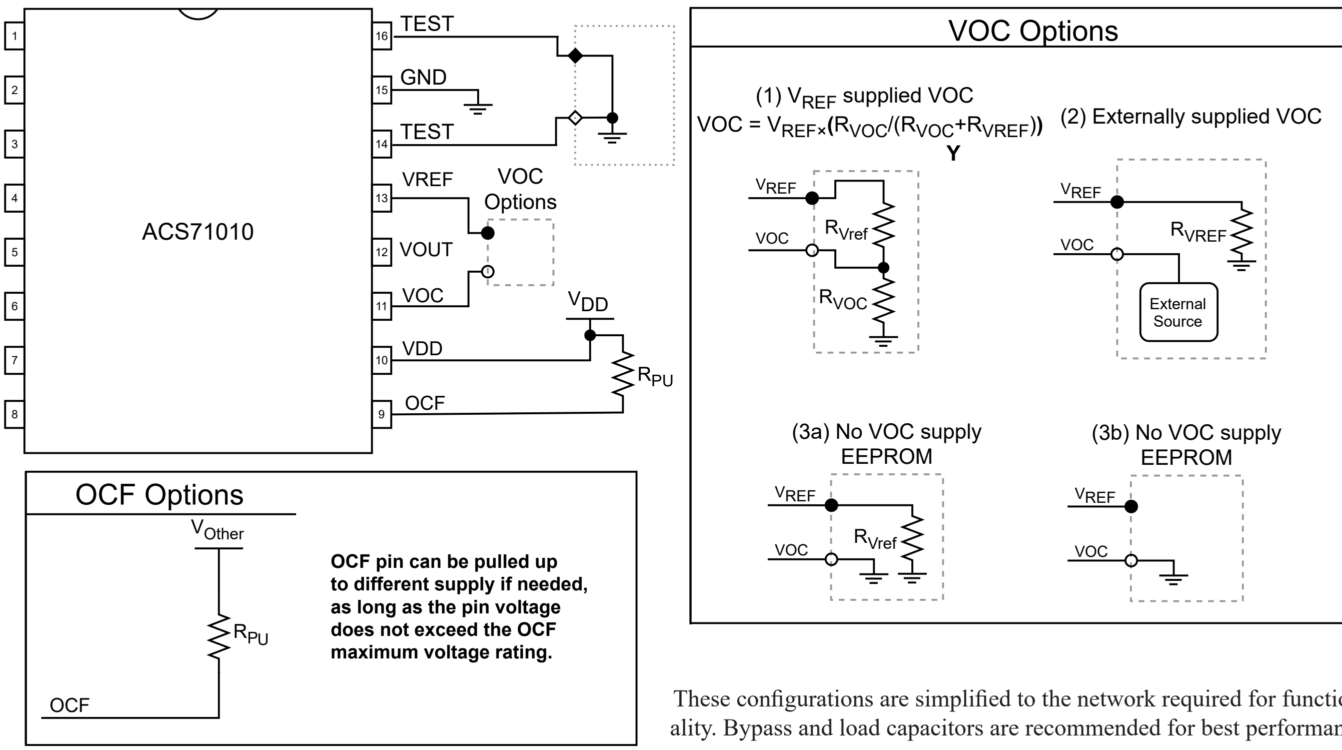
APPLICATION AND THEORY



These configurations are simplified to the network required for functionality. Bypass and load capacitors are recommended for best performance.

Figure 9: Applications Circuits for TEST, VOC, and FAULT pin

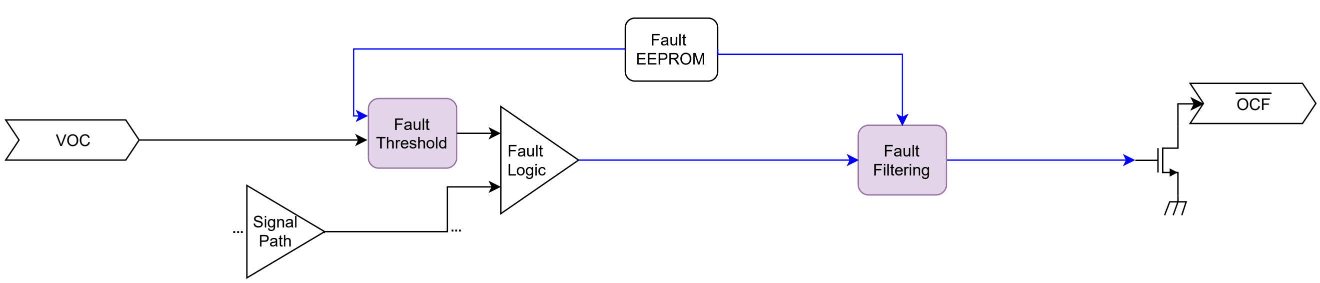


Figure 10: $\overline{\text{OCF}}$ Signal Path Simplified and Detailed Blocks of Functionality

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THERMAL PERFORMANCE

Resistive heating due to the flow of electrical current in the package should be considered during the thermal design of the application. The sensor, PCB, and PCB terminals generate heat and act as a heat sink.

The thermal response is highly dependent on the PCB layout, copper thickness, cooling method, and the profile of the injected current (including peak current, current on-time, and duty cycle).

In-pad vias help improve thermal performance. Placing vias under the copper pads of the board reduces electrical resistance and improves heat conduction to the PCB (Figure 11 and Figure 12). The ACSEVB-MA16-LA16 includes in-pad vias and is recommended to improve thermal performance.

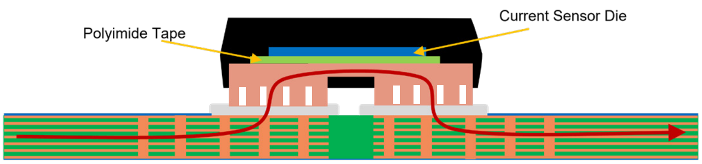

Figure 11: Vias Under Copper Pads (not to scale)

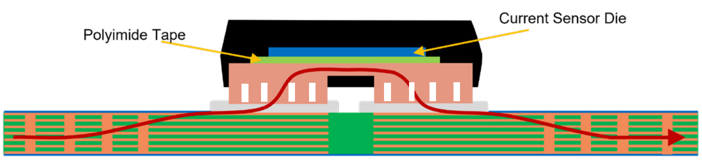

Figure 12: No Vias Under Copper Pads (not to scale)

Figure 13 shows the measured rise in steady-state die temperature of sensor versus DC continuous current at an ambient temperature T_A = 25°C for two board designs: with filled in-pad vias and without in-pad vias.

Figure 14 shows the measured rise in steady-state die temperature of sensor versus DC continuous current at ambient temperatures of 25°C and 125°C.

The thermal performance of sensor must always be verified in the specific conditions of the application. The maximum junction temperature of the sensor, T_{JMAX} = 165°C, must not be exceeded.

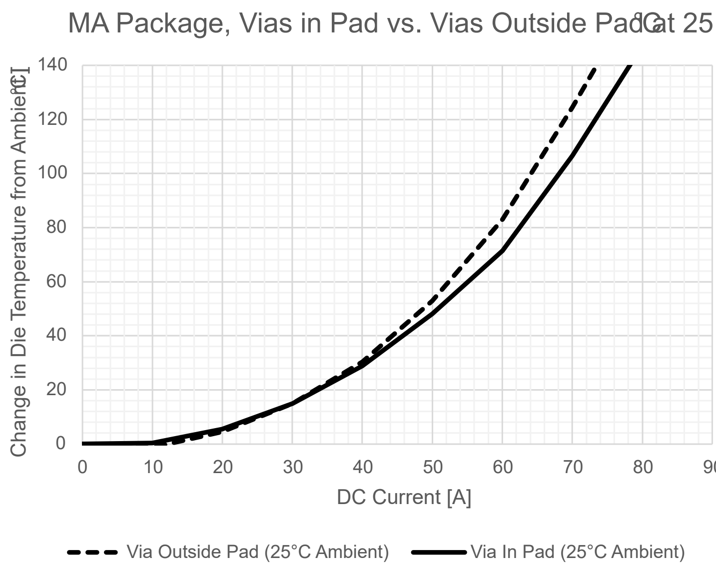

Figure 13: MA Package Performance with/without Vias

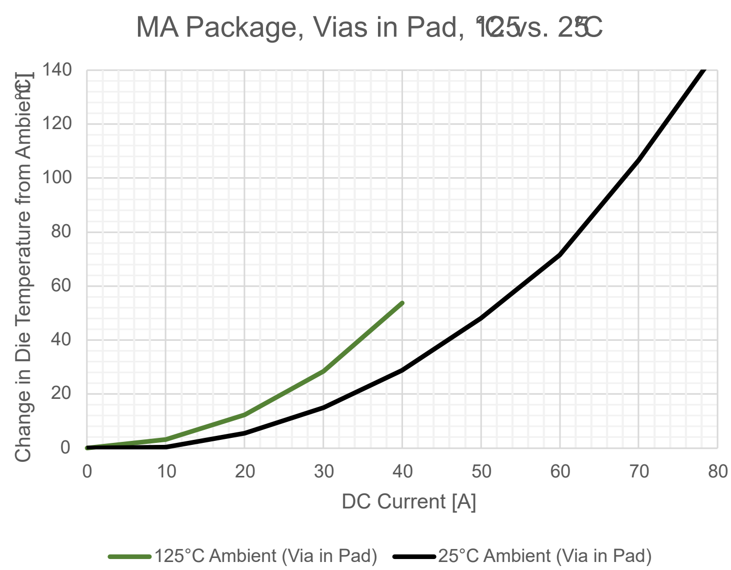

Figure 14: MA Package Performance at 25°C and 125°C

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Evaluation Board Layout

Thermal data shown was collected using the ACSEVB-MA16-LA16 Allegro evaluation board (TED-0004111). This board includes six layers of 2 oz. copper weight on all layers. The top and bottom layers of the PCB are shown in Figure 15.

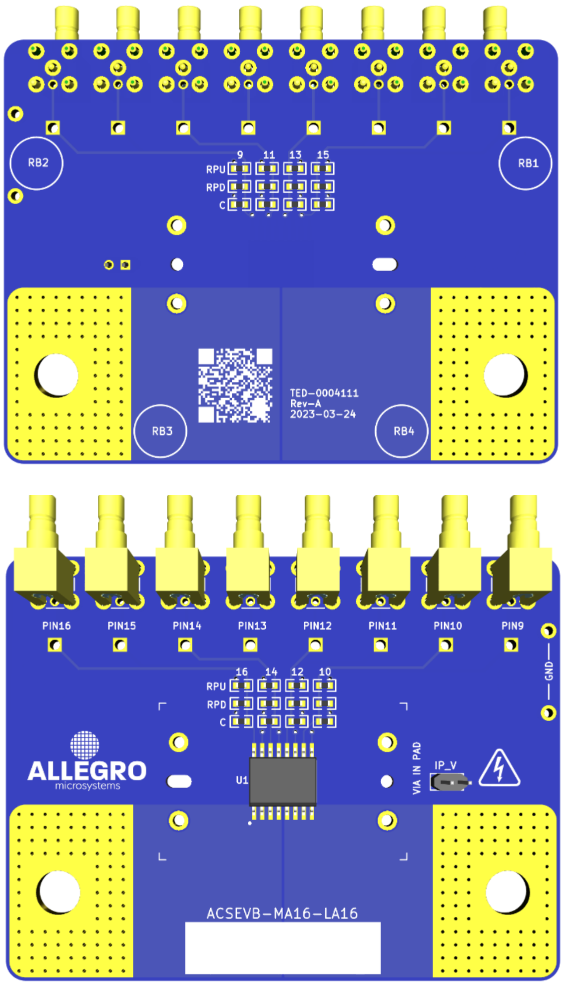

Figure 15: MA/LA Evaluation Board Top and Bottom Layers

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

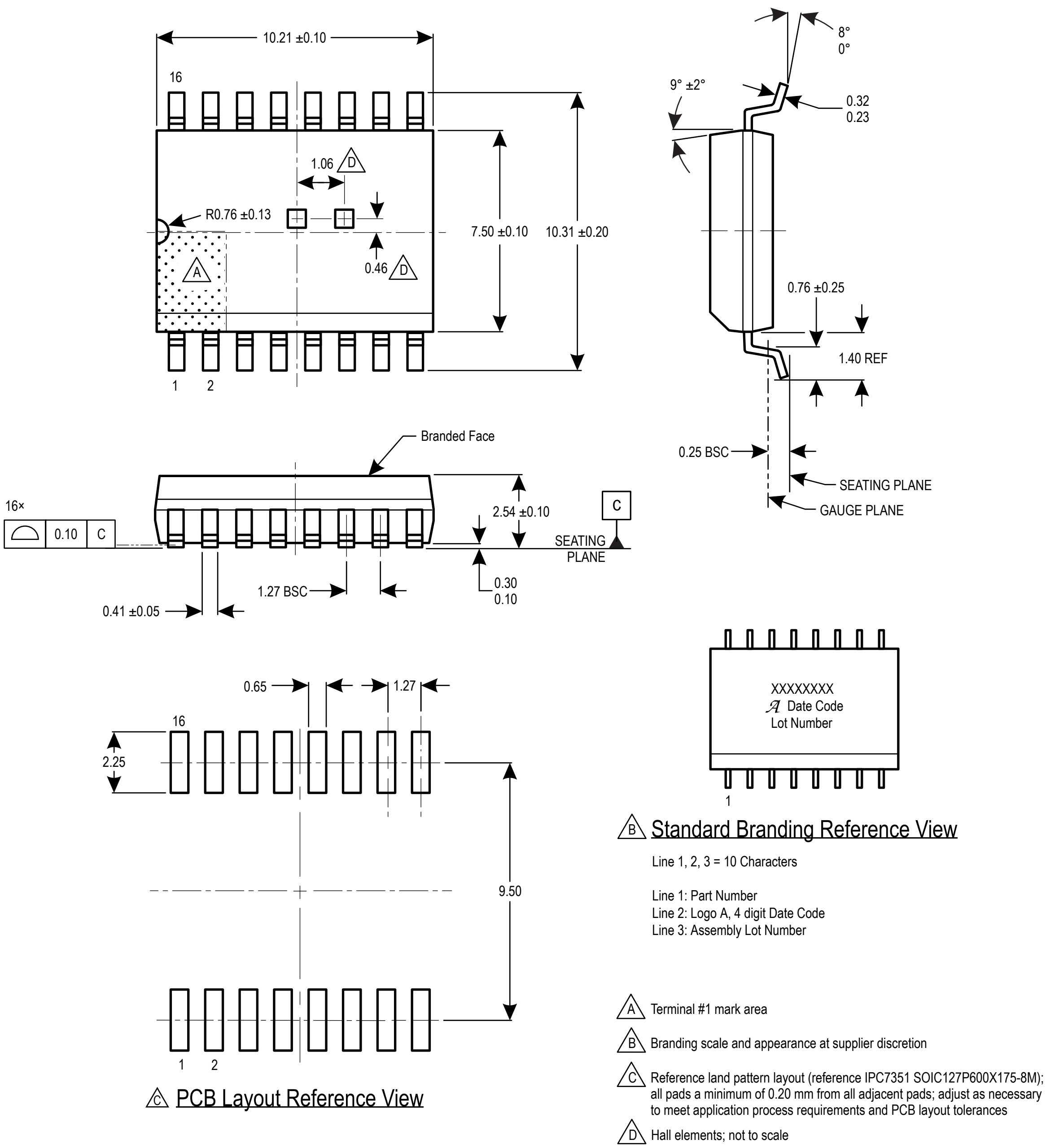

Figure 16: Package MA, 16-Pin SOICW

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REVISION HISTORY

Number	Date	Description
–	March 14, 2025	Initial release

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