NXP Semiconductors
Application Note

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MMPF0100 and MMPF0200 layout guidelines

1 Introduction

This document describes good practices for the layout of PF0100 and PF0200 devices on printed circuit boards. Though the guidelines are applicable to PF0100 and PF0200, reference is made only to the PF0100 throughout the document for simplicity.

Contents

2 Packaging

The PF0100 device is intended for use in commercial and industrial applications and is offered in a standard QFN for consumer and industrial applications. The PF0100Z is intended for use in automotive applications and is available in a Wettable-Flank QFN for automotive applications. Both packages are 56-pin and have an a 8 x 8 mm outline. Refer to Table 1 for the package drawing information for both packages.

Refer to Application Note AN1902 for guidelines on the handling and assembly of NXP QFN packages during PCB assembly, guidelines for PCB design and rework, and package performance information (such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical, and thermal resistance data).

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 1. Package drawing information

Product family	Package	Suffix	Package outline drawing number
MMPF0100	56 QFN 8x8 mm - 0.5 mm pitch. E-Type (full lead)	EP	98ASA00405D
MMPF0100Z	56 QFN 8x8 mm - 0.5 mm pitch. WF-Type (wettable flank)	ES	98ASA00379D
MMPF0200	56 QFN 8x8 mm - 0.5 mm pitch. E-Type (full lead)	EP	98ASA00405D

3 Recommended layer stack

Table 2 shows the recommended layer stack-up for the signals to receive good shielding.

Table 2. Layer stack-up recommendation

Layer	Stack-up
Layer 1 (Top)	Signal
Layer 2 (Inner 1)	Ground
Layer 3 (Inner 2)	Power
Layer 4 (Bottom)	Signal/Ground

Note: A more detailed layer design may be required to route the i.MX processor. If the PF0100 is being interfaced with an i.MX processor, just four of the layers will be needed to route it.

4 Component placement hints

Place these components as close as possible to the IC in order of priority:

- Input capacitor of the buck regulators (SW1, SW2, SW3, and SW4)
- Output diode and output capacitor of the boost converter (SWBST)
- VIN, VCOREREF, VCORE, and VCOREDIG capacitors
- LICELL capacitor (if a coin cell is used in system)
- VSNVS, VREFDDR, and VGENx capacitors
- Switching regulator inductors

5 General routing guidelines

- Shield feedback paths of the regulators from noise planes and traces
- The Exposed Pad (EP) on the PF0100 is the high current ground return for all the buck regulators and the boost regulator. Use vias under the EP to drop in directly onto the ground plane(s), ensuring sufficient copper for the ground return.
- Pins 14, 15, 32, and 48 are signal ground pins. Ground return currents from the switching regulators must not flow through these pins.
- The SWxIN, SWxLX, and SWBSTLX nodes are high dI/dt nodes and act as antennas. They are also high current paths. Hence their traces must be kept short and wide.
- Avoid coupling traces between important signal/low noise supplies (like VCOREREF) and switching nodes.

6 I^2C communication signals

To avoid contamination of these signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.

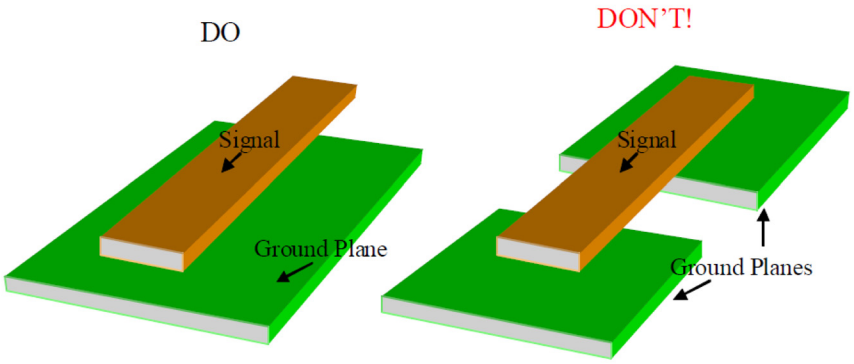

Figure 1. Recommended shielding for critical signals

7 Switching power supply traces

In the buck and boost configurations, length of the ‘critical traces’ must be kept minimal. ‘Critical traces’ refer to current paths which have high dI/dt. Refer to sections 7.1 and 7.2 for details.

7.1 Buck regulator

Figure 2 shows current paths in a buck converter in the ‘on’ and ‘off’ periods of the switching cycle. Critical traces refer to traces which conduct either only during the ‘on’, or only during the ‘off’ periods, as highlighted in red.

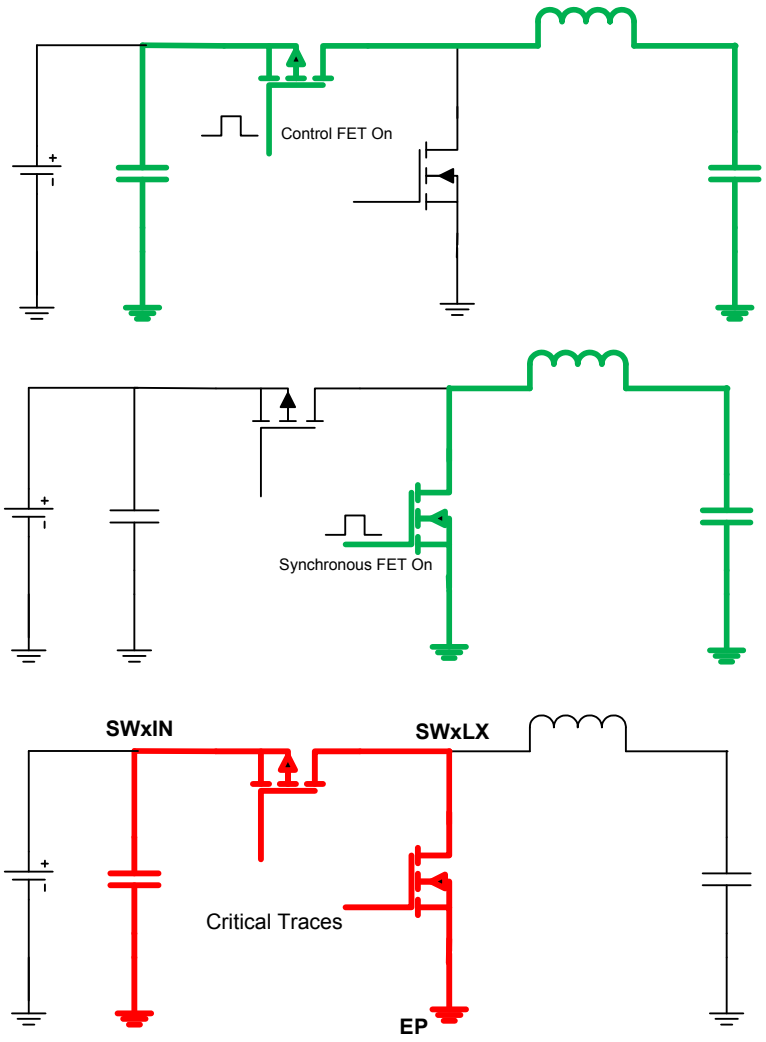

Figure 2. Buck converter critical traces

In the buck regulators of the PF0100, the top and bottom MOSFETs are integrated within the package. Hence, placement of the input capacitor close to the SWxIN pin and the exposed pad (EP) is critical. Figure 4 and Figure 5 show an example layout for the buck regulators.

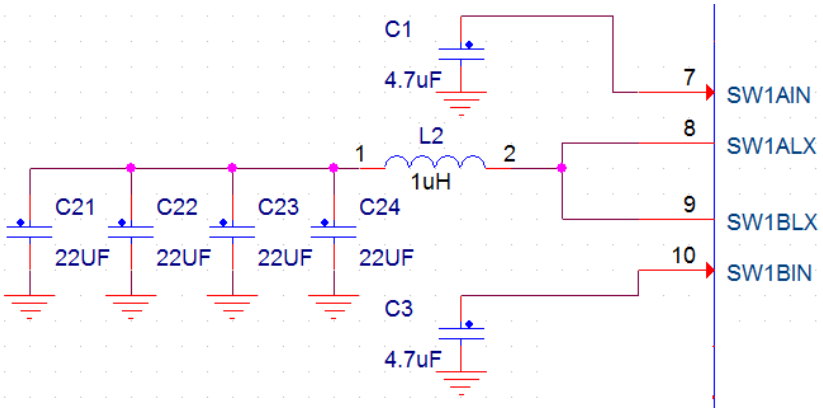

Figure 3. SW1AB schematic - reference for Figures 4 and 5

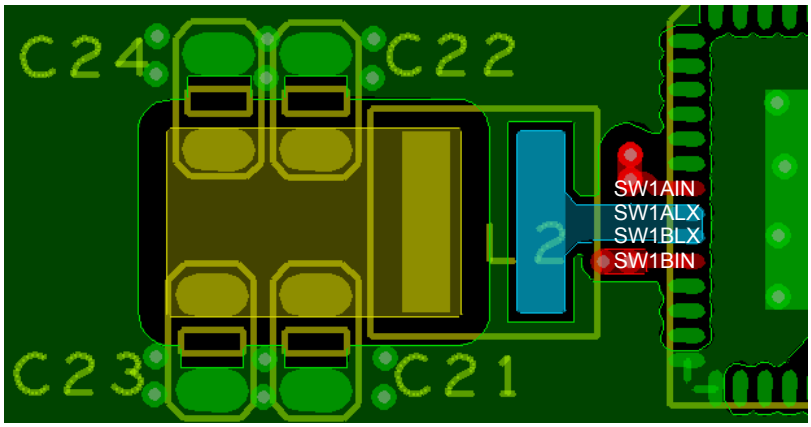

Figure 4. SW1AB layout - top layer components + top silkscreen

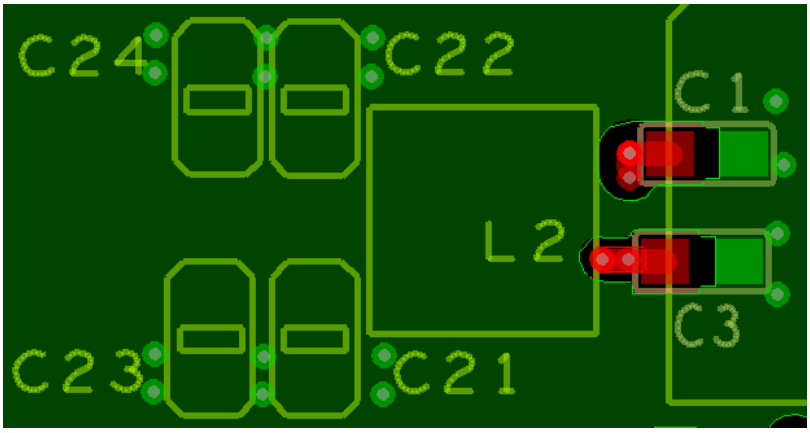

Figure 5. SW1AB layout - bottom layer components + top and bottom silkscreen

7.2 Boost converter

Figure 6 shows the critical traces in a boost converter.

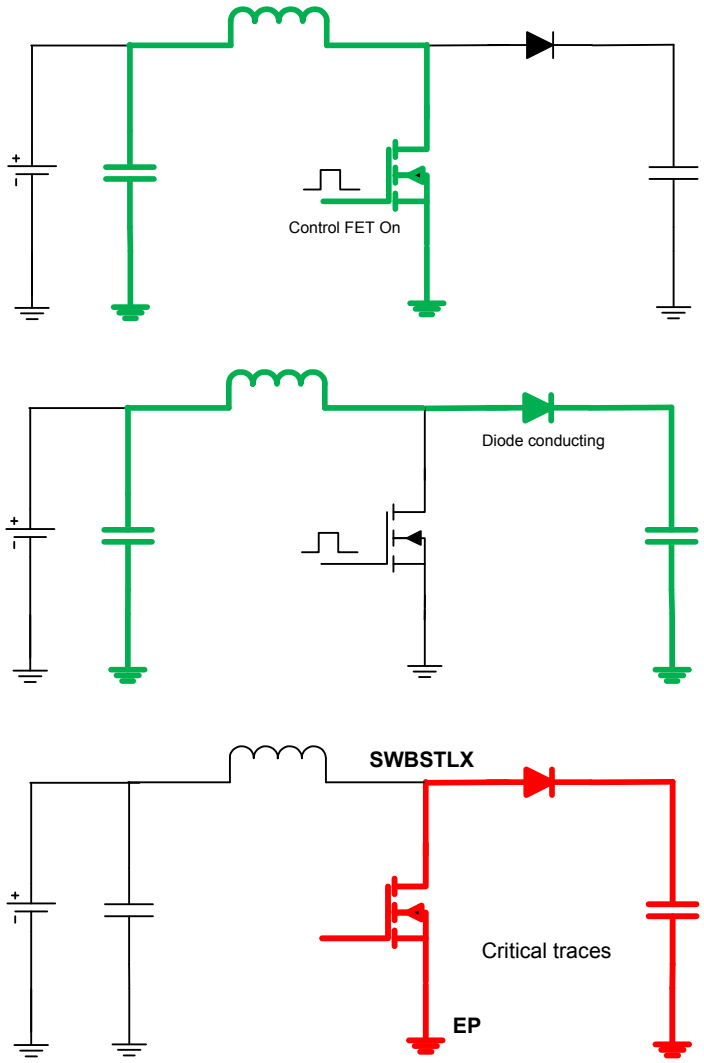

Figure 6. Boost converter critical traces

In the SWBST regulator of the PF0100, the switching MOSFET is integrated within the package. The loop formed by the switching MOSFET, the diode and the output capacitor, must be minimized to keep parasitic inductances small. Figure 8 and Figure 9 show an example of the SWBST layout.

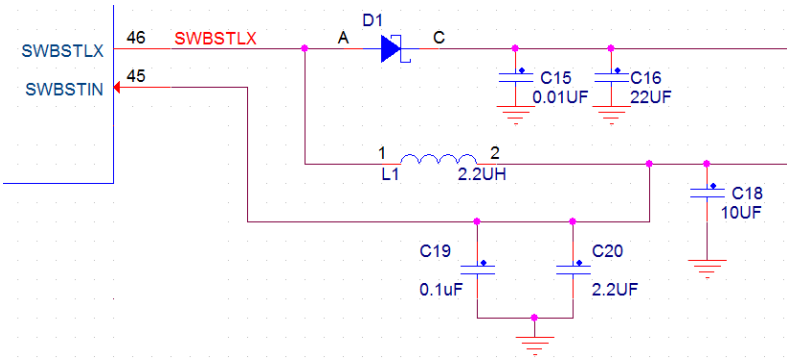

Figure 7. SWBST schematic - reference for Figures 8 and 9

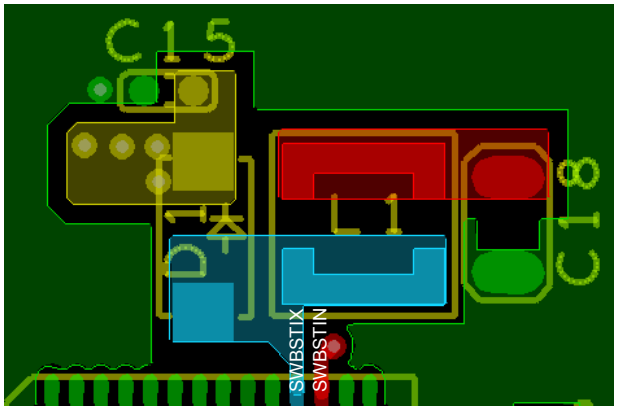

Figure 8. SWBST example layout. top layer components + top silkscreen

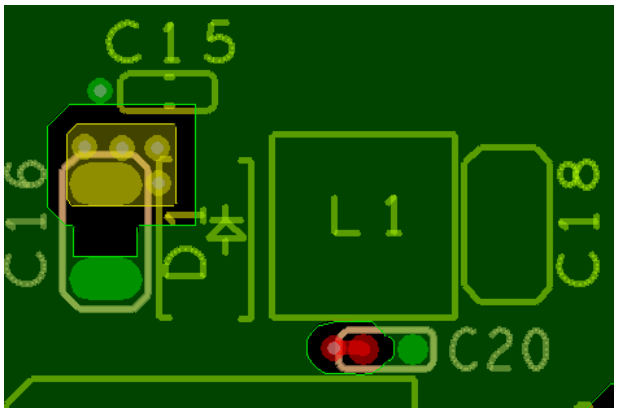

Figure 9. SWBST example layout. bottom layer components + top and bottom silkscreen

8 Effective grounding

- The practice of ‘star grounding’ must be followed for best performance of the PF0100.
- The exposed pad (EP) is the ground return for all the switching regulators and should be connected to the ground plane through multiple vias.
- SW1VSSSNS (pin 14), GNDREF1 (pin 15), SW3VSSSNS (pin 32), and GNDREF (pin 48) are signal ground pins. Connect these pins to the ground plane using separate vias not through EP, to prevent coupling from return currents of the switching regulators which pass through the EP.

9 Exposed pad connection

The exposed pad (EP) is the ground return for all the switching regulators and should be connected to the ground plane(s) through vias. A minimum of 16 vias is recommended under the EP. The EP also acts as a heat sink for the PF0100 hence the vias should not have thermal relief. They must be solid thermal vias as shown in Figure 10.

Figure 10. Types of via

‘Wicking’ of solder through the bore in the vias increase their thermal resistance. Follow techniques such as *tenting* or *via encroaching* to prevent solder wicking. Using a bore diameter of 0.3 mm or less also helps minimize wicking due to the surface tension of the liquid solder.

Apply the solder paste to approximately 50 to 75% of the area of the exposed pad. Rather than applying the solder paste in one large section, apply it in multiple smaller sections. This can be accomplished by using an array of openings in the solder stencil. Sectioning helps in even spreading of the solder, as well as in minimizing *out-gassing,* which can create voids and bridges under the exposed pad. Figure 11 shows an example of how the exposed pad can be laid out.

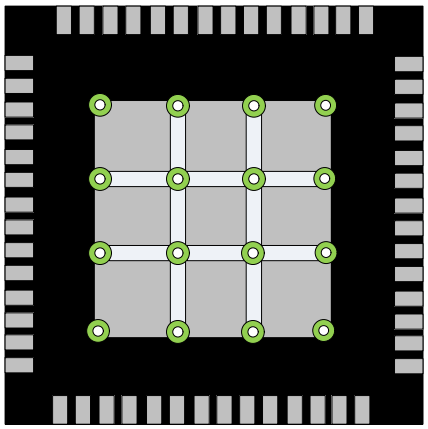

Figure 11. Exposed pad via array

10 Feedback signals

The control loop regulates output voltage at the point where the feedback trace meets the output rail. It is recommended to connect the feedback trace to the output voltage rail near the load for best load regulation. It must be ensured that this trace does not couple noise from other traces/layers.

11 References

Document number and description		URL
MMPF0100	Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MMPF0100.pdf
MMPF0200	Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MMPF0200.pdf
AN1902	QFN Application Note	http://www.nxp.com/files/analog/doc/app_note/AN1902.pdf
Support Pages		URL
MMPF0100 Product Summary Page		http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100
MMPF0200 Product Summary Page		http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MMPF0200
Power Management Home Page		http://www.nxp.com/webapp/sps/site/homepage.jsp?code=POWERMGTHOME
Analog Home Page		http://www.nxp.com/analog

12 Revision history

Revision	Date	Description of changes
2.0	11/2012	• Initial release
3.0	3/2013	• Deleted specific package drawings and ref in the table 1 to the 98A spec.
4.0	6/2013	• Added information on the MMPF0200
5.0	6/2015	• AN4530 is replaced by AN1902
	7/2016	• Updated to NXP document form and style

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