

NCN26010 - Retrieving and Applying a Globally Unique MAC Address

AND90175/D

Introduction

The NCN26010 10Base-T1S device is designed to meet IEEE 802.3cg specifications as well as the Open Alliance SPI protocol (TC6) with various optional additional features.

Network Protocol Stacks running on the Host will have to set a source MAC address. NCN26010 provides a globally unique MAC address that can be used for this purpose. This eliminates the need for users to obtain their own MAC address.

This application note describes how the MAC address is stored in the device, how it can be retrieved, and how MAC address filters can be set in NCN26010 to enable packet filtering using this globally unique MAC address.

Reference Documents

- [1] IEEE Std 802.3™ –2018
IEEE Standard for Ethernet
- [2] [NCN26010 datasheet](#)

OUI and MAC Address

The OUI is defined in [1]:

“1.4.366 Organizationally Unique Identifier (OUI): A 24-bit unique number that identifies a manufacturer or other organization. While an OUI may be used as a globally unique identifier on its own, its primary purpose is to be extended to form universally administered, globally unique MAC addresses or other extended globally-unique identifiers.”

In the sense of Ethernet, a MAC address consists of the 24-bit OUI and a 24-bit MAC-identifier, resulting in a 48-bit long MAC address as shown below:

Byte					
0	1	2	3	4	5
OUI			MACID		
MAC address					

OUI Storage Location

The NCN26010 stores the OUI in two different locations:

1. In the 32-bit PHYID register at MMS1, address 0x0001
2. In the 16-bit PHYID0 and PHYID1 registers, MMS0 address 0xFF02 and 0xFF03

Note that both locations contain a copy of the same OUI so that the user can decide which of the two locations to retrieve the OUI from.

Please see the NCN26010 datasheet for details.

MACID Storage Location

The 24-bit unique MACID is stored in two 16-bit registers inside the NCN26010, MACID0 and MACID1.

Please see the NCN26010 datasheet for details.

Obtaining the OUI

To form the unique MAC address, a host will have to read the content of the PHYID (or PHYID0 and PHYID1) register as well as the two MACID register MACID0 and MACID1.

The OUI stored in PHYID (and PHYID0/1 respectively) needs to undergo some bit operations when retrieving it from the NCN26010. For historical reasons, the OUI in the PHYID registers is stored in reverse bit order.

Clause 22.2.4.3.1 of [1], graphically explains the way the OUI is stored in the PHYID registers:

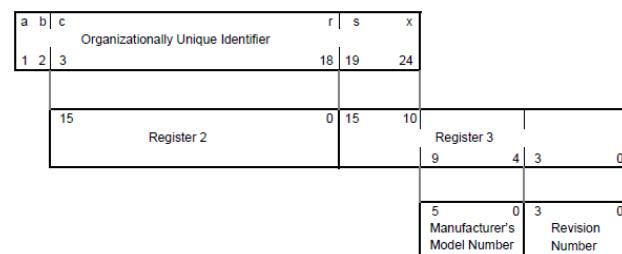


Figure 22-14—Format of PHY Identifier

Figure 1.

Note that in this context, Register 2 of the IEEE descriptions equals PHYID0 and register 3 equals PHYID1 of the NCN26010 device. The 32 bit PHYID register is a concatenation of PHYID0[15:0] and PHYID1[15:0] like shown below:

PHYID[31:0]															
PHYID0[15:0]								PHYID1[15:0]							

As shown in figure 22–14 of [1], the OUI's bits 3 to 18 are stored in register 2 (PHYID0), while bits 19 to 24 are stored in bits 15 down to 10 of Register 3 (PHYID1).

Note how the bits are stored in reversed order.

Alternatively, we can say the OUI's bits 3 to 24 are stored in bits 31 down to 10 of the PHYID register (MMS0 address 0x0001).

Also note that in the IEEE representation the LSB bit is designated as 1, while in computer programs LSB are usually represented by the number 0.

Bits 1 and 2 of the OUI are not stored because they have a special meaning:

Bit 1: when 1, denotes a multicast address. In the context of the OUI, this is always considered to be 0.

Bit 2: if 1, this means that the resulting MAC address (OUI and MACID) is managed locally and is therefore not guaranteed to be globally unique. This bit is also considered 0 in the OUI context.

Furthermore, bits 9 to 0 of the PHYID (or PHYID1) do not contribute to the OUI, but store the manufacturer number and the revision number (but not in reverse order as in the case of the OUI).

Let's assume we read 0x 180FF400 from PHYID register of the NCN26010. How can we determine the OUI?

	Bits																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYID	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	
	1				8				0				F				F				4				0				0			
OUI bit #	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24										
OUI	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1										

By adding 00 [bit 1 and bit 2] and then reversing the bit order, we get the OUI in this example:

Binary	1011	1111	1100	0000	0110	0000
HEX	B	F	6	0	C	0

Thus the three bytes of the OUI become:

OUI[0] : 0x60

OUI[1] : 0xC0

OUI[2] : 0xBF

Following is a simple piece of C-code, that illustrates how the OUI is determined using a computer or a Microcontroller:

```

void printOUI(uint32_t PHYID)
{
    uint16_t PHYID2 = PHYID >> 16;
    uint16_t PHYID3 = (uint16_t)PHYID & 0x0000FFFF;
    uint8_t OUI[3];
    printf("PHYID2 : %04x PHYID3: %04X ", PHYID2, PHYID3);
    // work on Byte 0
    uint8_t temp = (uint8_t)(PHYID2 >> 8) & 0x0FC;
    // printf("\temp %x\n", temp);
    //OUI[0] = 0;
    OUI[0] = ((temp >> 2) & 0x01) << 7;
    OUI[0] |= (temp >> 3 & 0x01) << 6;
    OUI[0] |= (temp >> 4 & 0x01) << 5;
    OUI[0] |= (temp >> 5 & 0x01) << 4;
    OUI[0] |= (temp >> 6 & 0x01) << 3;
    OUI[0] |= (temp >> 7 & 0x01) << 2;
    printf("OUI: %02x:", OUI[0]);
    // get Byte 1
    temp = (uint8_t)(PHYID2 >> 2) & 0x00FF;
    OUI[1] = (temp & 0x01) << 7;
    OUI[1] |= (temp >> 1 & 0x01) << 6;
    OUI[1] |= (temp >> 2 & 0x01) << 5;
    OUI[1] |= (temp >> 3 & 0x01) << 4;
    OUI[1] |= (temp >> 4 & 0x01) << 3;
    OUI[1] |= (temp >> 5 & 0x01) << 2;
    OUI[1] |= (temp >> 6 & 0x01) << 1;
    OUI[1] |= (temp >> 7 & 0x01);
    printf("%02x:", OUI[1]);
    temp = (uint8_t)(PHYID3 >> 10) & 0xFF;
    OUI[2] = (temp & 0x01) << 7;
    OUI[2] |= (temp >> 1 & 0x01) << 6;
    OUI[2] |= (temp >> 2 & 0x01) << 5;
    OUI[2] |= (temp >> 3 & 0x01) << 4;
    OUI[2] |= (temp >> 4 & 0x01) << 3;
    OUI[2] |= (temp >> 5 & 0x01) << 2;
    temp = (uint8_t)(PHYID2 & 0x03);
    //printf ("temp : %d\n",temp);
    OUI[2] |= (temp & 0x01) << 1;
    OUI[2] |= (temp >> 1 & 0x01);
    printf("%02x\n", OUI[2]);
}

// extra home work: extract the Model Number and Chip Revision
uint8_t ModelNumber = (uint8_t)(PHYID >> 4) & 0x3F;
uint8_t ChipRev = (uint8_t)(PHYID & 0x0000000F);
printf("Model Number : %d Chip Rev: %d\n", ModelNumber, ChipRev);
}

```

Figure 2.

Forming the MAC Address

Now that the OUI is retrieved, the MAC address can simply be formed as shown in the table below:

MAC[0]	MAC[1]	MAC[2]	MAC[3]	MAC[4]	MAC[5]
OUI[0]	OUI[1]	OUI[2]	MACID1[7:0]	MACID0[15:8]	MACID0[7:0]

As an example, assume MACID0 to be 0x000000203 and MACID1 to be 0x00000001, with the OUI from above the resulting MAC address would result in: 60:C0:BF:01:02:03

Once retrieved, the MAC address can now be set as the source MAC address in the host running the upper layer of the network stack. The MAC address also be used to filter incoming ethernet packet for the matching destination address inside the MACPHY.

This helps to reduce the number of interrupt requests generated by the NCN26010, since Ethernet packets whose destination address does not match the MAC address of the host are directly discarded by the hardware in the NCN26010 and thus do not have to be delivered to the host.

For details on how to configure the MAC filters inside the NCN26010 please see the datasheet and the “getting started” Application note [AND90155/D](#).

onsemi, **ONSEMI**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION**LITERATURE FULFILLMENT:**Email Requests to: orderlit@onsemi.com**TECHNICAL SUPPORT****North American Technical Support:**Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative