MIC2810

Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low V_{IN} LDOs

Features

- 2.7V to 5.5V Input Voltage Range
- 2 MHz DC/DC Converter and Two LDOs
- Integrated Power-on Reset (POR)
- Adjustable POR Delay Time
- LOWQ Mode
  - 30 µA Total I_Q When in LOWQ Mode
- DC/DC Converter
  - Up to 600 mA of Output Current in PWM Mode
  - LOWQ Mode: No Ripple Light Load Mode
  - 53 μV_{RMS} Output Noise in LOWQ Mode
  - 2 MHz PWM Mode Operation
  - >90% Efficiency
- LDO1
  - 1.65V to 5.5V Input Voltage Range
  - 300 mA Output Current
  - Output Voltage Down to 0.8V
- LDO2
  - 2.7V to 5.5V Input Voltage Range
  - 300 mA Output Current
  - Output Voltage Down to 0.8V
- Thermal Shutdown Protection
- Current-Limit Protection
- Simple, Leakage-Free Interfacing to Host MPU in Applications with Backup Power
- Tiny 16-Pin 3 mm x 3 mm QFN Package

Applications

- Embedded MPU and MCU Power
- Portable and Wearable Applications
- Low-Power RF Systems
- Backup Power Systems

General Description

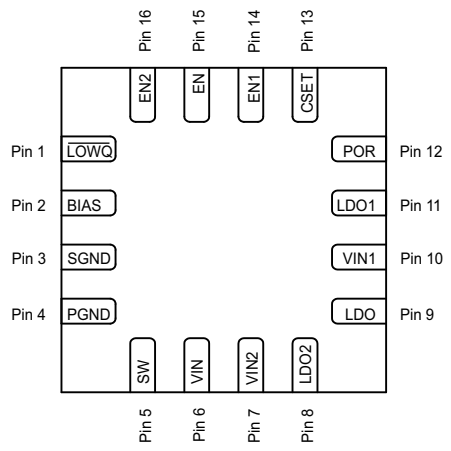
The MIC2810 is a high performance power management IC, featuring three output voltages with independent enable control: a 2 MHz DC/DC converter and two 300 mA LDOs. The MIC2810 features a LOWQ mode, reducing the total current draw while in this mode to less than 30 µA. In LOWQ mode, the output noise of the DC/DC converter is 53 μV_{RMS}, significantly lower than other converters that use a PFM light load mode that can interfere with sensitive RF circuitry.

The DC/DC converter uses small values of L and C to reduce board space but still retains high efficiency over a wide load range, while supporting load currents up to 600 mA.

The LDOs operate with very small ceramic output capacitors for stability, therefore, reducing required board space and component cost. It is available in various output voltage options in the 16-pin 3 mm x 3 mm QFN leadless package.

Package Type

MIC2810
16-PIN 3 mm x 3 mm QFN



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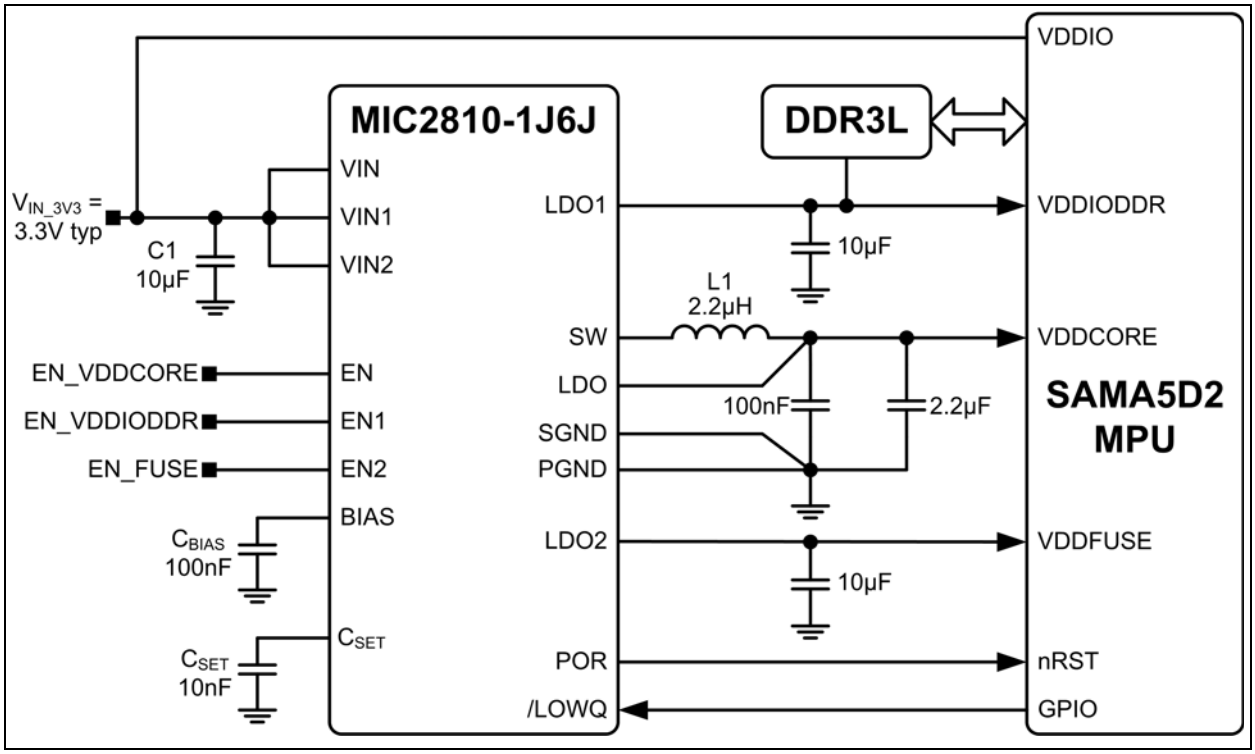
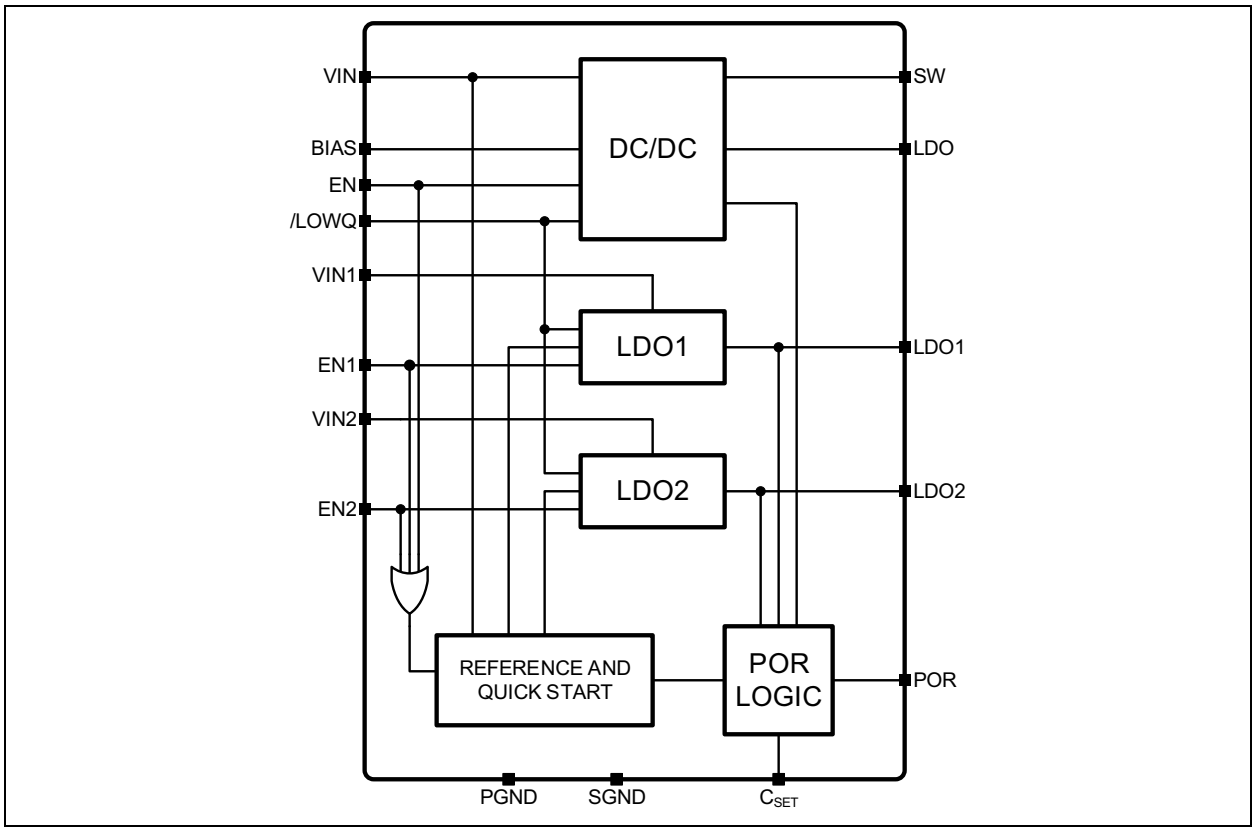
Typical Application Circuit (simplified)



Functional Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}, V_{IN1}, V_{IN2}) ..... 0V to +6.0V
Enable Input Voltage (V_{EN}, V_{EN1}, V_{EN2}) ..... 0V to V_{IN}
Power Dissipation (Note 1) ..... Internally Limited
ESD Rating (Note 2) ..... 2 kV

Operating Ratings ‡

Supply Voltage (V_{IN}, V_{IN2}) ..... +2.7V to +5.5V
Supply Voltage (V_{IN1}) ..... +1.65V to +5.5V
Enable Input Voltage (V_{EN}, V_{EN1}, V_{EN2}) ..... 0V to +V_{IN}

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V_{IN} = EN1 = EN2 = $\overline{LOWQ}$ = V_{OUT} (Note 2) + 1V; $C_{OUTDC/DC}$ = 2.2 µF, C_{LDO1} = C_{LDO2} = 2.2 µF; $I_{OUTDC/DC}$ = 100 mA; $I_{OUTLDO1}$ = $I_{OUTLDO2}$ = 100 µA; T_J = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
UVLO Threshold	$UVLO_{TH}$	**2.45**	2.55	**2.65**	V	Rising input voltage during turn-on
UVLO Hysteresis	$UVLO_{HYS}$	—	100	—	mV	—
Ground Pin Current	I_{GND}	—	800	1100	µA	V_{FB} = GND (not switching)
		—	55	85		LDO1 or LDO2 (EN = GND; EN1 or EN2 = GND)
		—	—	**95**		
Ground Pin Current in Shutdown	I_{GND_SHDN}	—	0.2	5	µA	EN = EN1 = EN2 = 0V
Ground Pin Current (LOWQ mode)	I_{GND_LOWQ}	—	30	60	µA	All channels on, $I_{DC/DC}$ = I_{LDO1} = I_{LDO2} = 0 mA ($\overline{LOWQ}$ = GND)
		—	—	**80**		
		—	20	**70**		LDO1 or LDO2 (EN = GND; EN1 or EN2 = GND); I_{OUT} = 0 mA ($\overline{LOWQ}$ = GND)
Overtemperature Shutdown	T_{SD}	—	160	—	°C	—
Overtemperature Shutdown Hysteresis	T_{SDHYS}	—	23	—	°C	—
Enable Inputs (EN; EN1; EN2; $\overline{LOWQ}$)						
Enable Input Voltage	V_{IH}	—	—	**0.2**	V	Logic Low
	V_{IL}	**1.0**	—	—	V	Logic High
Enable Input Current	I_{ENLK}	—	0.1	**1**	µA	V_{IL} ≤ 0.2V
		—	0.1	**1**	µA	V_{IH} ≥ 1.0V
Turn-on Time						
Turn-on Time (LDO1 and LDO2)	$t_{TURN-ON}$	—	240	**500**	µs	—
Turn-on Time (DC/DC)	$t_{TURN-ON}$	—	83	**350**	µs	($\overline{LOWQ}$ = V_{IN}; I_{LOAD} = 300 mA); ($\overline{LOWQ}$ = GND; I_{LOAD} = 10 mA)
POR Output						
POR Threshold Voltage, Falling	V_{THLOW_POR}	90	91	—	%	Low Threshold, % of nominal ($V_{DC/DC}$ or V_{LDO1} or V_{LDO2}) (Flag ON)
POR Threshold Voltage, Rising	V_{THIGH_POR}	—	96	99	%	High Threshold, % of nominal ($V_{DC/DC}$ and V_{LDO1} and V_{LDO2}) (Flag OFF)
VOL	VOL_{POR}	—	10	**100**	mV	POR Output Logic Low Voltage; I_L = 250 µA
IPOR	$ILEAK_{POR}$	—	0.01	**1**	µA	Flag Leakage Current, Flag OFF
SET INPUT						
SET Pin Current Source	I_{SET}	0.75	1.25	1.75	µA	V_{SET} = 0V
SET Pin Threshold Voltage	VTH_{SET}	—	1.25	—	V	POR = High

Note 1: Specification for packaged product only.

2: V_{OUT} denotes the highest of the three output voltages of DC/DC, LDO1 and LDO2.

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TABLE 1-2: ELECTRICAL CHARACTERISTICS - DC/DC CONVERTER

Electrical Characteristics: $V_{IN} = V_{OUTDC/DC} + 1V$; EN1 = V_{IN}; EN2 = GND; $I_{OUTDC/DC}$ = 100 mA; L = 2.2 µH; $C_{OUTDC/DC}$ = 2.2 µF; T_J = 25°C, **bold** values indicate –40°C to + 125°C; unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
LOWQ = High (Full Power Mode)						
Output Voltage Accuracy	V_{OUT}	–2	—	2	%	Nominal V_{OUT} tolerance
		–3	—	**3**		
Output Voltage Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	—	0.2	—	%/V	V_{OUT} > 2.4V; $V_{IN} = V_{OUT}$ + 300 mV to 5.5V, I_{LOAD}= 100 mA V_{OUT} < 2.4V; V_{IN} = 2.7V to 5.5V, I_{LOAD}= 100 mA
Output Voltage Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.1	—	%	20 mA < I_{LOAD} < 600 mA
Maximum Duty Cycle	DC_{MAX}	100	—	—	%	$V_{FB} \leq 0.4V$
PWM Switch ON-Resistance	—	—	0.5	—	Ω	I_{SW} = 150 mA, $V_{FB} = 0.7V_{FB_NOM}$ PMOS
		—	0.6	—	Ω	I_{SW} = –150 mA, $V_{FB} = 1.1V_{FB_NOM}$ NMOS
Oscillator Frequency	f_{osc}	**1.8**	2	**2.2**	MHz	—
Current Limit in PWM Mode	—	0.75	1	1.6	A	$V_{FB} = 0.9 * V_{NOM}$
LOWQ = Low (Light Load Mode)						
Output Voltage Accuracy	V_{OUT}	–2	—	2	%	Variation from nominal V_{OUT}
		–3	—	**3**		Variation from nominal V_{OUT}; –40°C to +125°C
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	—	0.02	0.3	%/V	$V_{IN} = V_{OUT}$ + 1V to 5.5V; I_{OUT} = 100 µA
		—	—	**0.6**		
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.4	1.5	%	I_{OUT} = 100 µA to 50 mA
Ripple Rejection	PSRR	—	45	—	dB	f = up to 1 kHz
Current Limit	I_{LIM_LOWQ}	80	120	190	mA	V_{OUT} = 0V
Output Voltage Noise	V_N	—	53	—	μV_{RMS}	10 Hz to 100 kHz

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TABLE 1-3: ELECTRICAL CHARACTERISTICS - LDO1/LDO2

Electrical Characteristics: $V_{IN1} = V_{IN2} = V_{OUTLDO1} + 1.0V$ or $V_{IN1} = V_{IN2} = V_{OUTLDO2} + 1.0V$; EN = GND; EN1 = EN2 = $V_{IN1} = V_{IN2}$; $C_{LDO1} = C_{LDO2} = 2.2\ \mu F$; $I_{OUTLDO1} = 100\ \mu A$; $T_J = 25°C$, **bold** values indicate $-40°C \le T_J \le +125°C$; unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
LOWQ = High (Full Power Mode)						
Output Voltage Accuracy	V_{OUT}	–2	—	2	%	Variation from nominal V_{OUT}
		–3	—	**3**		Variation from nominal V_{OUT}; –40°C to +125°C
Line Regulation	—	—	0.02	0.3	%/V	$V_{IN} = V_{OUT}$ +1V to 5.5V
		—	—	**0.6**		
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.20	—	%	I_{OUT} = 100 µA to 150 mA
		—	0.25	—		I_{OUT} = 100 µA to 200 mA
		—	0.40	**1.5**		I_{OUT} = 100 µA to 300 mA
Dropout Voltage	V_{DO}	—	70	—	mV	I_{OUT} = 150 mA
		—	94	—		I_{OUT} = 200 mA
		—	142	**300**		I_{OUT} = 300 mA
Ripple Rejection	PSRR	—	35	—	dB	f = up to 1 kHz
Current Limit	I_{LIM}	400	600	850	mA	V_{OUT} = 0V
Output Voltage Noise	V_N	—	91	—	μV_{RMS}	10 Hz to 100 kHz
LOWQ = Low (Light Load Mode)						
Output Voltage Accuracy	V_{OUT}	–3	—	3	%	Variation from nominal V_{OUT}
		–4	—	**4**		Variation from nominal V_{OUT}; –40°C to +125°C
Line Regulation	—	—	0.02	0.3	%/V	$V_{IN} = V_{OUT}$ +1V to 5.5V
		—	—	**0.6**		
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	**1.0**	%	I_{OUT} = 100 µA to 10 mA
Dropout Voltage	V_{DO}	—	22	35	mV	I_{OUT} = 10 mA
		—	—	**50**		
Current Limit	I_{LIM}	50	85	125	mA	V_{IN} = 2.7V; V_{OUT} = 0V
Ripple Rejection	PSRR	—	35	—	dB	f = up to 1 kHz

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TABLE 1-4: TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Junction Temperature	T_J	–40	—	+125	°C	—
Package Thermal Resistance						
16-Ld QFN	θ_{JA}	—	56	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

For this page only, DC/DC Normal Mode ($\overline{LOWQ}$ = V_{IN})

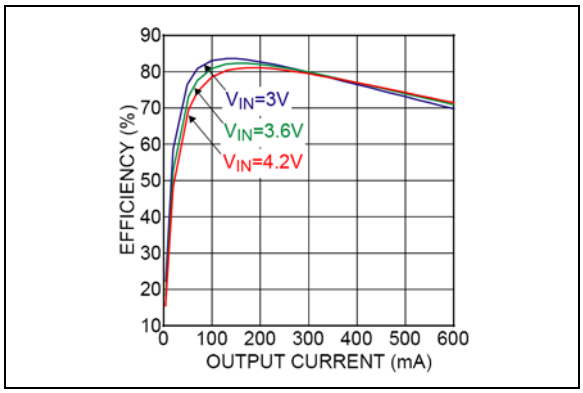

FIGURE 2-1: *1.2V_{OUT} Efficiency.*

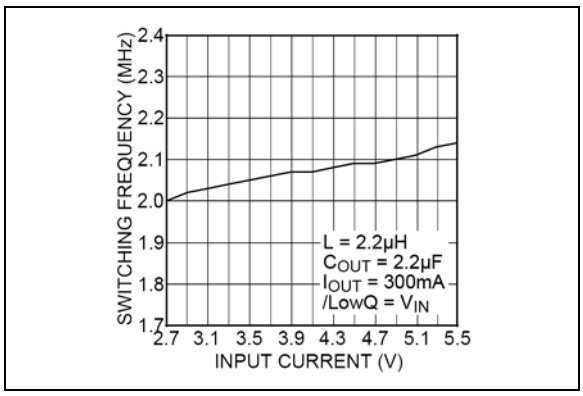

FIGURE 2-2: *Switching Frequency vs. Input Voltage.*

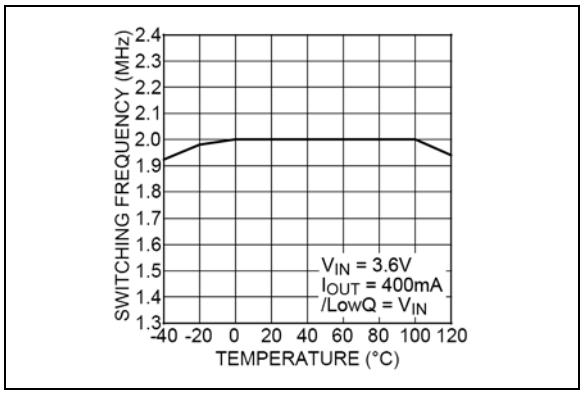

FIGURE 2-3: *Switching Frequency vs. Temperature.*

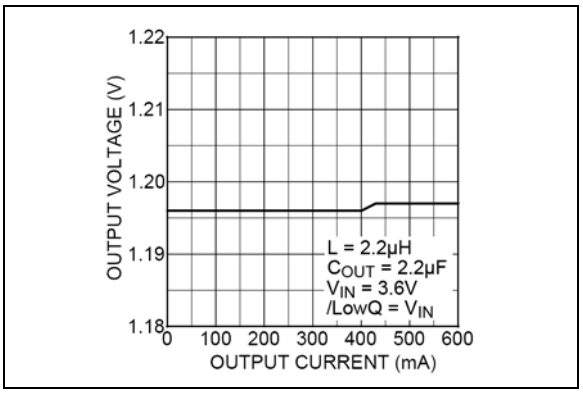

FIGURE 2-4: *Load Regulation.*

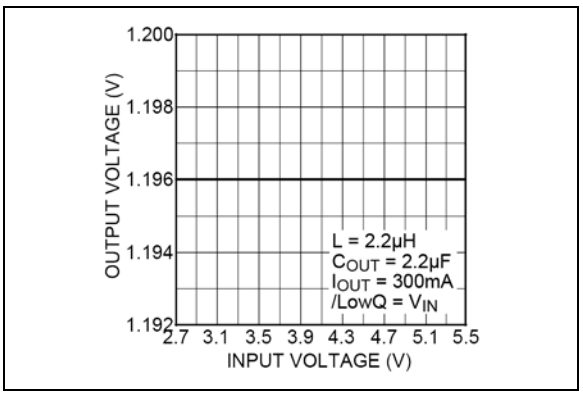

FIGURE 2-5: *Line Regulation.*

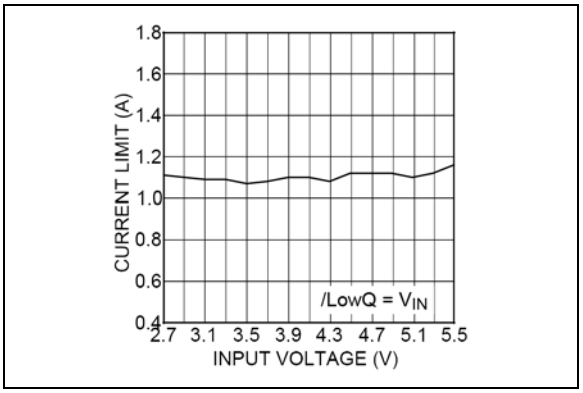

FIGURE 2-6: *Current Limit vs. Input Voltage.*

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For this page only, DC/DC LOWQ Mode ($\overline{LOWQ}$ = GND)

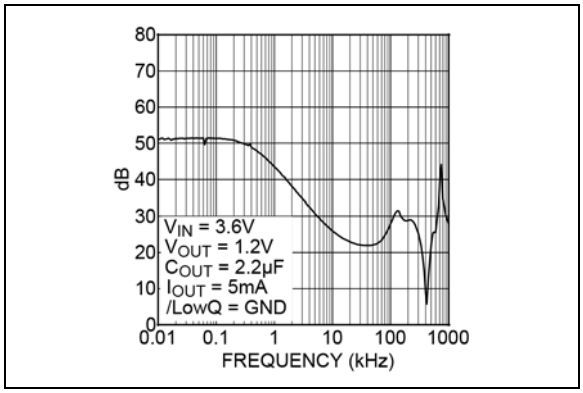

FIGURE 2-7: *Power Supply Rejection Ratio.*

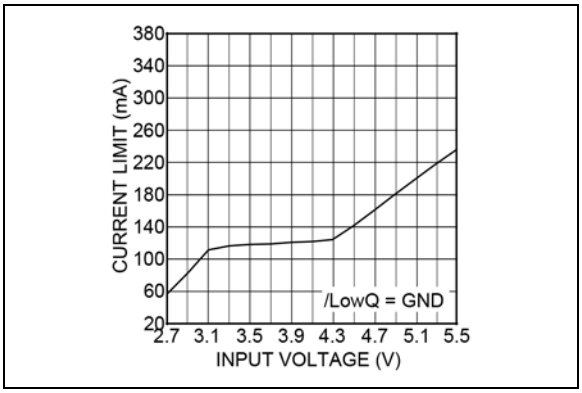

FIGURE 2-10: *Current Limit vs. Input Voltage.*

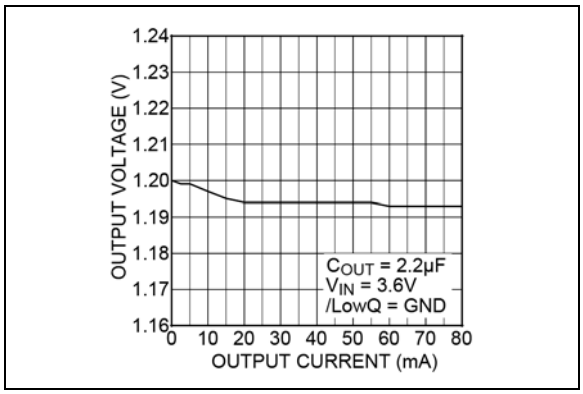

FIGURE 2-8: *Load Regulation.*

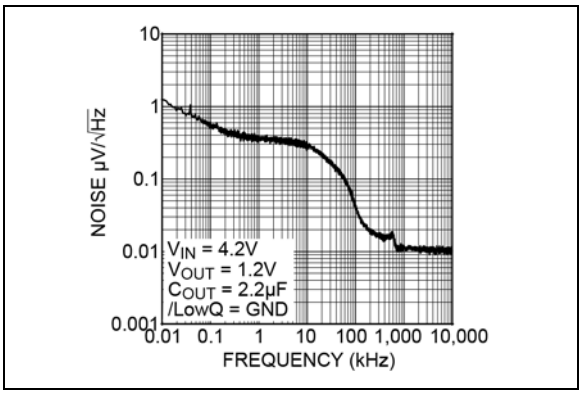

FIGURE 2-11: *Output Noise Spectral Density.*

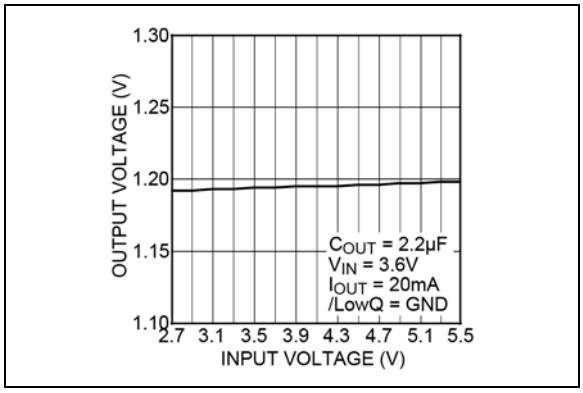

FIGURE 2-9: *Line Regulation.*

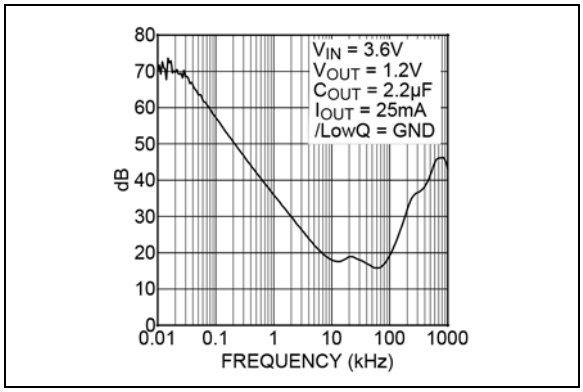

FIGURE 2-12: *Power Supply Rejection Ratio LDO1 (LOWQ Mode).*

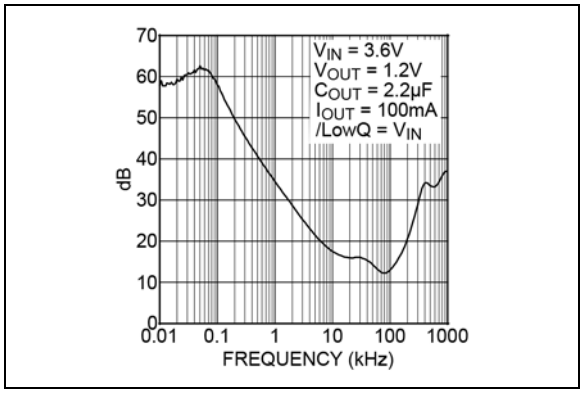

FIGURE 2-13: *Power Supply Rejection Ratio LDO1 (Normal Mode).*

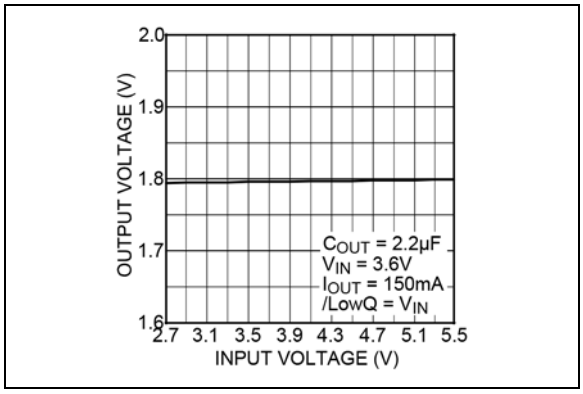

FIGURE 2-14: *LDO1 Line Regulation.*

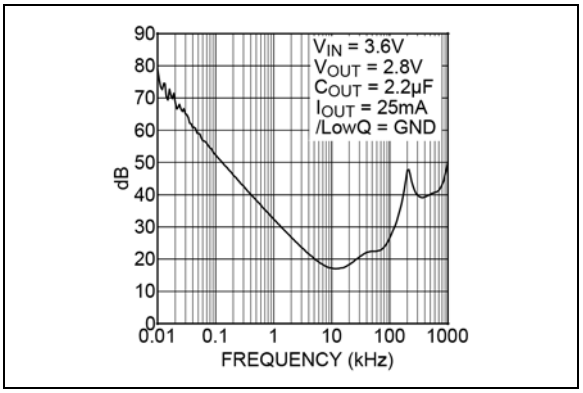

FIGURE 2-15: *Power Supply Rejection Ratio LDO2 (LOWQ Mode).*

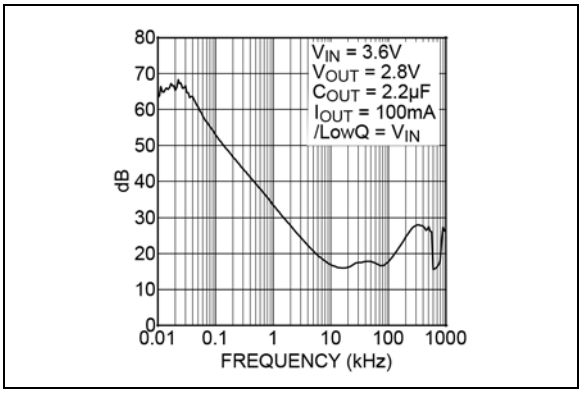

FIGURE 2-16: *Power Supply Rejection Ratio LDO2 (Normal Mode).*

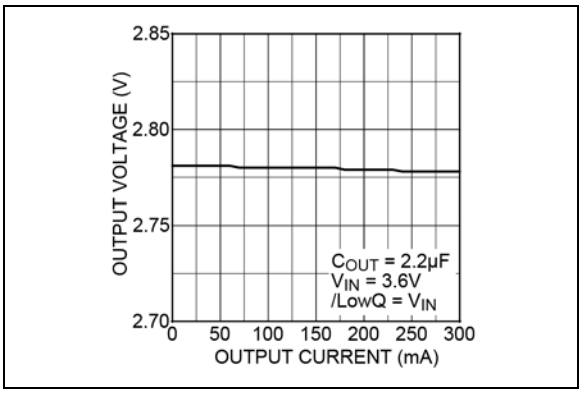

FIGURE 2-17: *LDO2 Load Regulation.*

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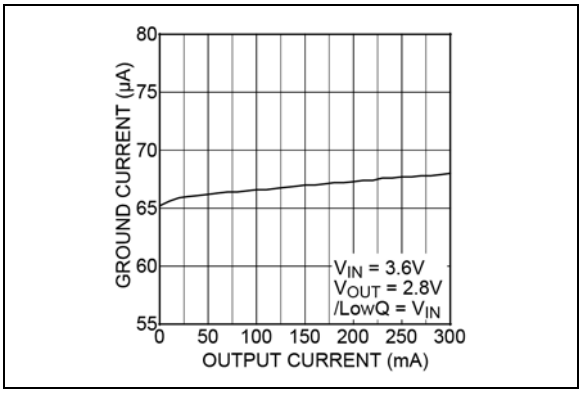

FIGURE 2-18: *LDO2 Ground Current vs. Output Current.*

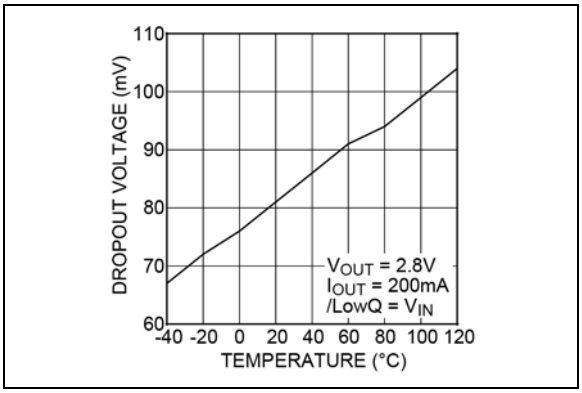

FIGURE 2-21: *LDO2 Dropout Voltage vs. Temperature.*

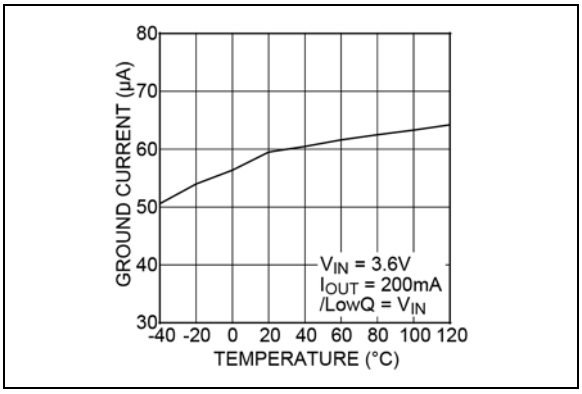

FIGURE 2-19: *LDO2 Ground Current vs. Temperature.*

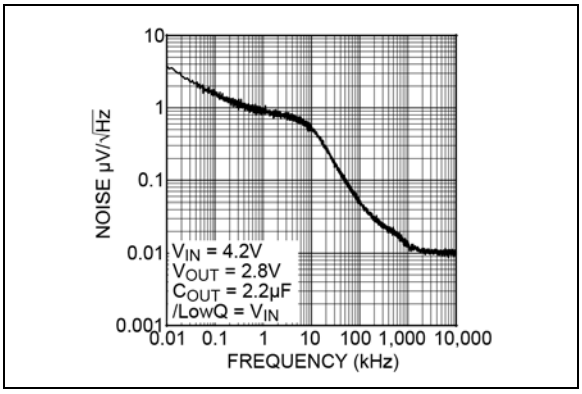

FIGURE 2-22: *LDO2 Output Noise Spectral Density.*

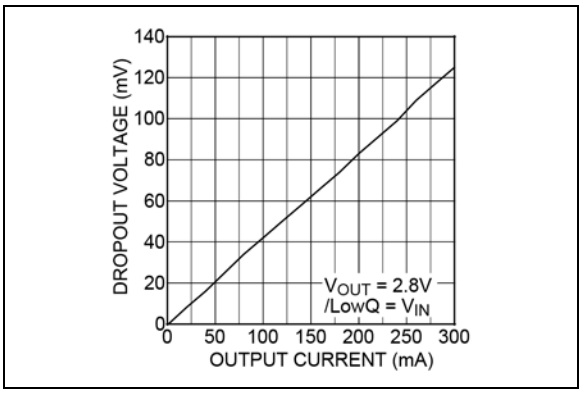

FIGURE 2-20: *LDO2 Dropout Voltage vs. Output Current.*

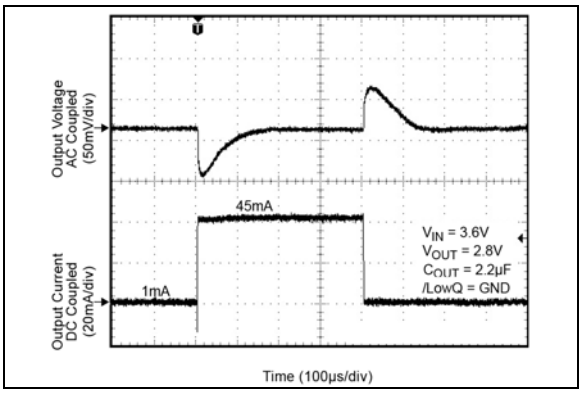

FIGURE 2-23: *LDO2 (LOWQ Mode) Load Transient.*

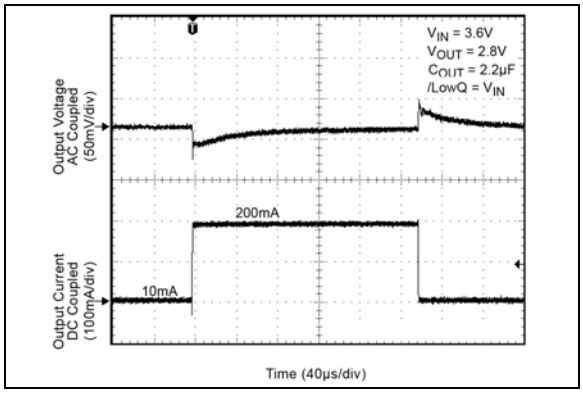

FIGURE 2-24: *LDO2 (Normal Mode) Load Transient.*

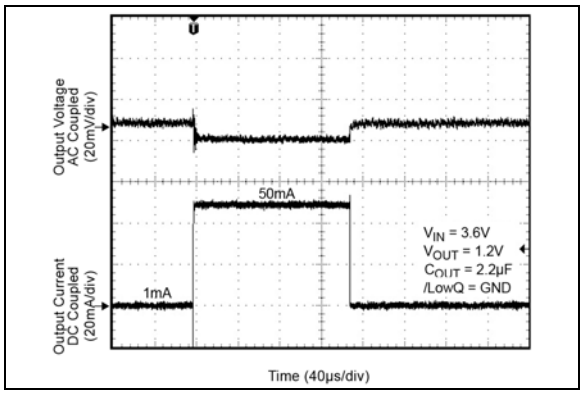

FIGURE 2-25: *DC/DC (LOWQ Mode) Load Transient.*

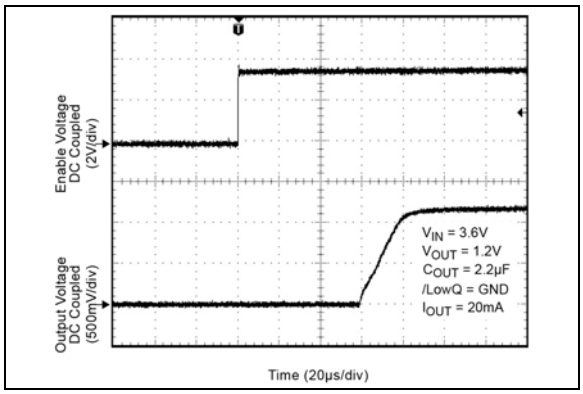

FIGURE 2-26: *DC/DC (LOWQ Mode) Start-Up Waveform.*

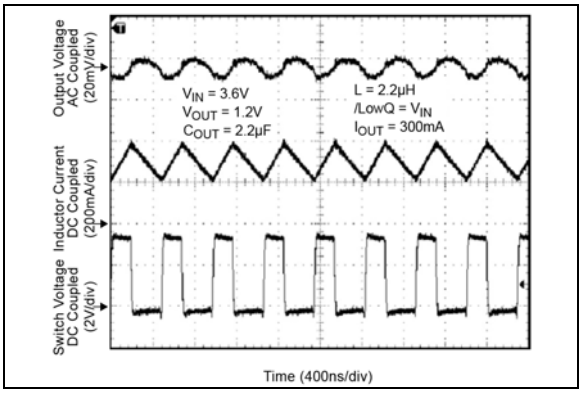

FIGURE 2-27: *DC/DC PWM Waveforms.*

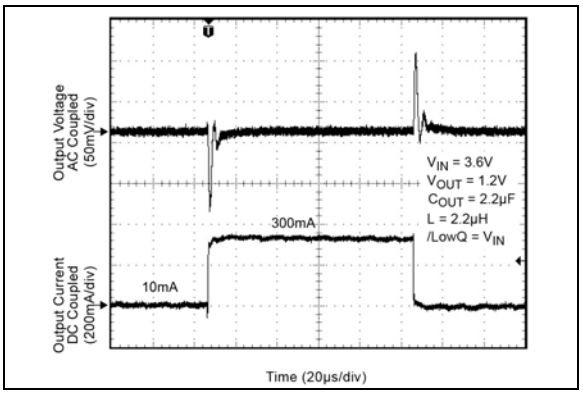

FIGURE 2-28: *DC/DC Load Transient.*

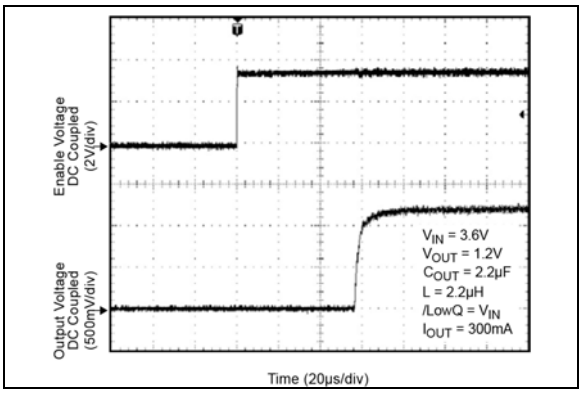

FIGURE 2-29: *DC/DC Start-Up Waveforms.*

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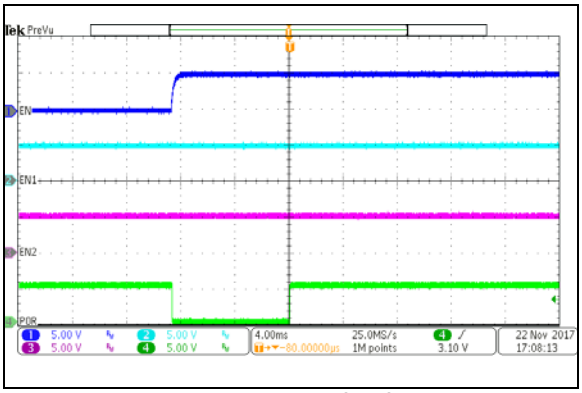

FIGURE 2-30: *POR Behavior; EN1 = EN2 = High, Low-to-High Transition on EN.*

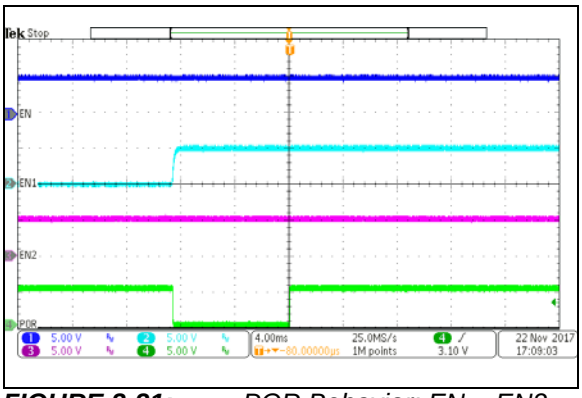

FIGURE 2-31: *POR Behavior; EN = EN2 = High, Low-to-High Transition on EN1.*

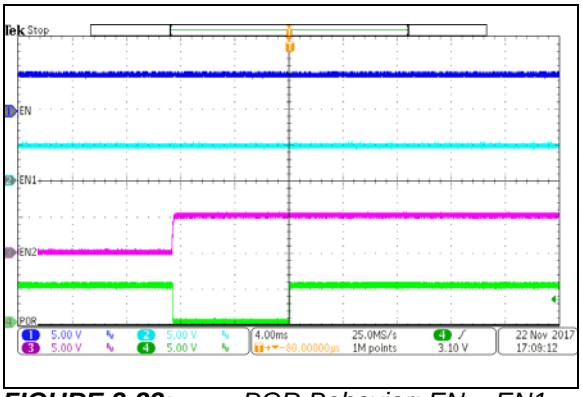

FIGURE 2-32: *POR Behavior; EN = EN1 = High, Low-to-High Transition on EN2.*

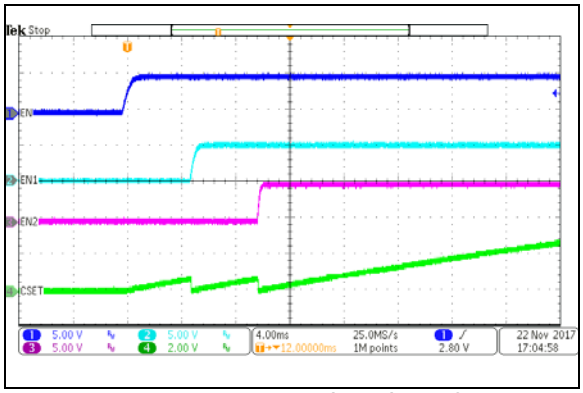

FIGURE 2-33: *C_{SET} Pin Voltage for Correct Sequencing.*

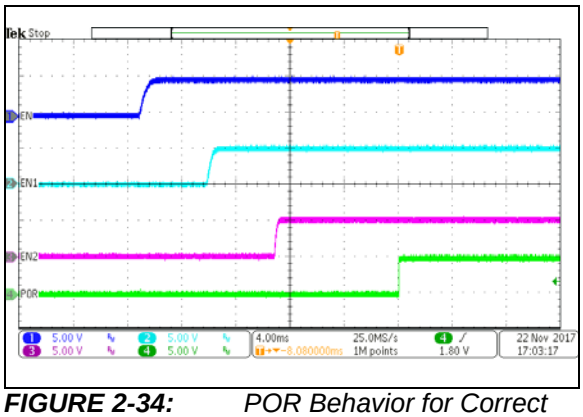

FIGURE 2-34: *POR Behavior for Correct Sequencing.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	$\overline{LOWQ}$	LOWQ Mode. Active Low Input. Logic High = Full Power Mode; Logic Low = LOWQ Mode; Do not leave floating.
2	BIAS	Internal circuit bias supply. It must be decoupled to signal ground with a 0.1 µF capacitor and should not be loaded.
3	SGND	Signal ground.
4	PGND	Power ground.
5	SW	Switch (Output): Internal power MOSFET output switches.
6	V_{IN}	Supply Input – DC/DC and other circuitry shared with LDO1 and LDO2. Must be connected to Pin 7.
7	V_{IN2}	Supply Input – LDO2. Must be connected to Pin 6.
8	LDO2	Output of LDO regulator 2.
9	LDO	LDO Output: Connect to V_{OUT} of the DC/DC for LOWQ mode operation.
10	V_{IN1}	Supply Input – LDO1.
11	LDO1	Output of LDO regulator 1.
12	POR	Power-on Reset Output: Open-drain output. Active low indicates an output undervoltage condition on either one of the three regulated outputs.
13	C_{SET}	Delay Set Input: Connect external capacitor to GND to set the internal delay for the POR output. When left open, there is a minimum delay. This pin cannot be grounded.
14	EN1	Enable Input (LDO1). Active High Input. Logic high = On; Logic low = Off; do not leave floating.
15	EN	Enable Input (DC/DC). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.
16	EN2	Enable Input (LDO2). Active High Input. Logic high = On; Logic low = Off; do not leave floating.

3.1 $\overline{LOWQ}$

The $\overline{LOWQ}$ pin provides a logic level control between the internal PWM switching regulator mode, and the low noise linear regulator mode. With $\overline{LOWQ}$ pulled low (≤ 0.2V), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical supply current of 38 µA. In linear (LDO) mode, the output can deliver 60 mA of current to the output. By placing $\overline{LOWQ}$ high (≥ 1V), the device transitions into a constant frequency PWM step-down regulator mode. This allows the device the ability to efficiently deliver up to 600 mA of output current at the same output voltage.

LOWQ mode also limits the output load of both LDO1 and LDO2 to less than 50 mA.

3.2 BIAS

The BIAS pin supplies the power to the internal control and reference circuitry. The bias is powered from V_{IN} through an internal 6Ω resistor. A small 0.1 µF capacitor is required for bypassing.

3.3 SGND

Signal ground (SGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be as small as possible.

3.4 PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible.

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3.5 SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

3.6 $V_{IN}/V_{IN1}/V_{IN2}$

Three input voltage pins provide power to the switch mode regulator, LDO1, and LDO2. V_{IN} provides power to the control circuitry of the DC/DC converter and voltage reference circuitry shared by all the regulators in the MIC2810. LDO1's input voltage (V_{IN1}) can go down to 1.65V, but LDO2 and the DC/DC converter input voltages are limited to 2.7V minimum.

For the switch mode regulator, V_{IN} provides power to the MOSFET along with current limiting sense circuitry. Due to the high switching speeds, a 4.7 µF capacitor is recommended close to V_{IN} and the power ground (PGND) pin for bypassing. Please refer to the PCB layout section for an example of an appropriate circuit layout.

3.7 LDO2

Regulated output voltage of LDO2. Power is provided by V_{IN2}. The minimum recommended output capacitance is 2.2 µF.

3.8 LDO

The LDO pin is the output of the linear regulator and should be connected to the output of the step-down PWM regulator. In LOWQ mode ($\overline{LOWQ}$ < 0.2V), the LDO provides the output voltage of the DC/DC regulator.

3.9 LDO1

Regulated output voltage of LDO1. Input power is provided by V_{IN1}. The minimum recommended output capacitance is 2.2 µF.

3.10 Power-on Reset (POR)

The power-on reset output is an open-drain N-Channel device, requiring a pull-up resistor to either the input voltage or output voltage for proper voltage levels. The POR output has a delay time that is programmable with a capacitor from the CSET pin to ground. The delay time can be programmed to be as long as 1 second. In steady-state conditions, the POR output is high if at least one channel (DC/DC, LDO1, and LDO2) is enabled and has reached regulation. This is equivalent to performing a logic OR operation on the status of the output voltages.

If any of the outputs are subsequently pulled out of regulation (e.g., due to a momentary overload), the POR signal goes low and it remains low as long as the affected output is out of regulation. If the affected output returns within regulation, POR is asserted high after the delay time programmed with the capacitor at the CSET pin.

The ESD protection of the POR pin is free from clamping diodes to the input supply rails. Therefore, the POR signal can be asserted to host I/Os under backup power domains or pulled up to backup power sources without the risk of parasitic leakage, even if the main power to the MIC2810 is removed.

3.11 C_{SET}

The CSET pin is a current source output that charges a capacitor that sets the delay time for the power-on reset output from low to high. The delay for POR high to low (detecting an undervoltage on any of the outputs) is always minimal. The current source of 1.25µA charges a capacitor up from 0V. When the capacitor reaches 1.25V, the output of the POR is allowed to go high. The delay time in microseconds is equal to the C_{SET} in picofarads.

EQUATION 3-1:

$$PORDelay(\mu s) = C_{SET}(pF)$$

3.12 EN/EN1/EN2

All enable inputs are active high, requiring 1.0V for guaranteed operation. EN provides logic control for the DC/DC regulator. EN2 provides logic control for LDO2, and EN1 provides logic control for LDO1. The enable inputs are CMOS logic and cannot be left floating.

The enable pins provide logic level control of the specified outputs. When all enable pins are in the off state, supply current of the device is greatly reduced (typically <1 µA). When the DC/DC regulator is in the off state, the output drive is placed in a "tri-stated" condition, where both the high side P-channel MOSFET and the low-side N-channel are in an “off” or non-conducting state. Do not drive any of the enable pins above the supply voltage.

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4.0 APPLICATION INFORMATION

The MIC2810 is a power management IC with a single integrated step-down regulator and two low dropout regulators. LDO1 and LDO2 are 300 mA low dropout regulators supplied from the input voltage pins. The step-down regulator is a 600 mA PWM power supply. All three regulators utilize a LOWQ light load mode to maximize battery efficiency under light load conditions. This is achieved with a $\overline{\text{LOWQ}}$ control pin that, when pulled low, shuts down all the biasing and drive current for the PWM regulator, along with reducing the current limit of the two independent LDOs. When the $\overline{\text{LOWQ}}$ pin is pulled low, the MIC2810 draws only 30 µA of operating current. This mode allows the output to be regulated through the LDO output, which is capable of providing 60 mA of output current. This method has the advantage of producing a clean, low current, ultra-low noise output in LOWQ mode. During LOWQ mode, the SW node becomes high impedance, blocking current flow. Other methods of reducing quiescent current, such as pulse frequency modulation (PFM) or bursting techniques create large amplitude and low frequency ripple voltages that can be detrimental to system operation.

When more than 60 mA is required, the $\overline{\text{LOWQ}}$ pin can be forced high, causing the MIC2810 to enter PWM mode. In this case, the LDO output makes a "hand-off" to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off allowing up to 600 mA of current to be efficiently supplied through the PWM output to the load.

4.1 Output Capacitor

LDO1 and LDO2 outputs require a 2.2 µF ceramic output capacitor for stability. The DC/DC switch mode regulator also requires a 2.2 µF ceramic output capacitor to be stable. All output capacitor values can be increased to improve transient response, but performance has been optimized for a 2.2 µF ceramic on the LDOs and the DC/DC regulator. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X5R/X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% to 60% respectively over their operating temperature ranges.

4.2 Input Capacitor

A minimum 1 µF ceramic, 4.7 µF recommended, should be placed as close as possible to the V_{IN} pin for optimal bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended. A minimum 1 µF is recommended close to the V_{IN} and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to the PCB layout section for an example of an appropriate circuit layout.

4.3 Inductor Selection

The MIC2810 is designed for use with a 2.2 µH inductor. Proper selection should ensure the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

EQUATION 4-1:

$$I_{PK} = I_{OUT} + \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \times f \times L}$$

Where:

I_{PK} = Peak inductor current.
I_{OUT} = Output/load current.
V_{IN} = Input voltage.
V_{OUT} = Output voltage.
f = Switching frequency of the PWM regulator.
L = Inductor value.

4.4 POR Delay Time

The POR signal also goes low for the duration of the delay time given by Equation 3-1 when only one of the enable inputs (EN, EN1, EN2) transitions from low to high, with the others being already high and the corresponding output being in regulation. This is shown in Figure 2-30, Figure 2-31, and Figure 2-32. At the low-to-high transition of either enable input, the CSET pin capacitor is discharged to ground, and the POR delay time is restarted.

At start-up, in order to prevent a momentary HIGH glitch of the POR signal between subsequent enable commands, it is recommended to set the POR delay time longer than the maximum delay expected between the enable command signals plus the turn-on time $t_{TURN\text{-}ON}$.

For a given delay between the enable signals, an example of correct POR delay time design is shown in Figure 2-33 and Figure 2-34. In Figure 2-33, it can be seen that the C_{SET} voltage is reset to ground by subsequent low-to-high enable signals transitions before it reaches the VTH_{CSET} voltage (1.25V typ.), thus extending the duration of the POR LOW assertion (Figure 2-34).

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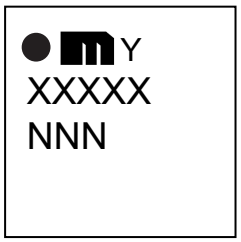
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

16-Pin QFN*



Part Number	Code
MIC2810-1JGMYML-TR	D1JGM
MIC2810-1J6JYML-TR	D1J6J
MIC2810-1J6SYML-TR	D1J6S
MIC2810-44MYML-TR	YD44M
MIC2810-4GKYML-TR	YD4GK
MIC2810-4GMYML-TR	YD4GM
MIC2810-4GPYML-TR	YD4GP
MIC2810-4GSYML-TR	YD4GS
MIC2810-4LSYML-TR	YD4LS
MIC2810-4MSYML-TR	YD4MS
MIC2810-CGJYML-TR	YDCGJ
MIC2810-FGSYML-TR	YDFGS

Refer to the Product Identification System section for information on the output voltage for each device.

Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

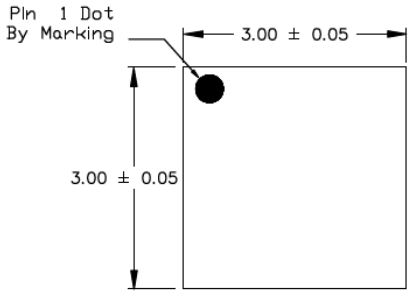
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

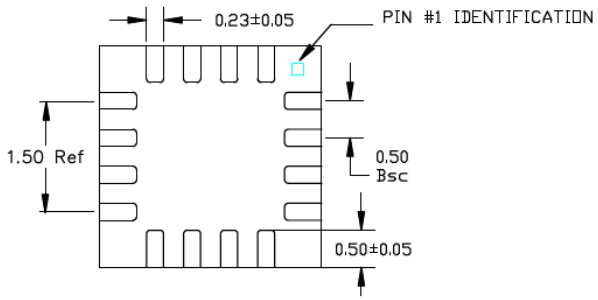
16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

TITLE
16 LEAD QFN 3.0x3.0mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

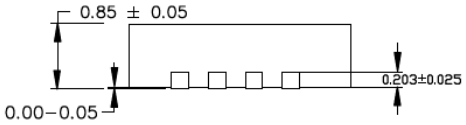
DRAWING #	CQFN33-16LD-PL-1	**UNIT**	MM
Lead Frame	NiPdAu	**Lead Finish**	NiPdAu



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
   N IS THE TOTAL NUMBER OF TERMINALS.
2. MAX PACKAGE WARPAGE IS 0.05mm, MAX ALLOWABLE BURRS IS 0.076 mm
   IN ALL DIRECTIONS.
3. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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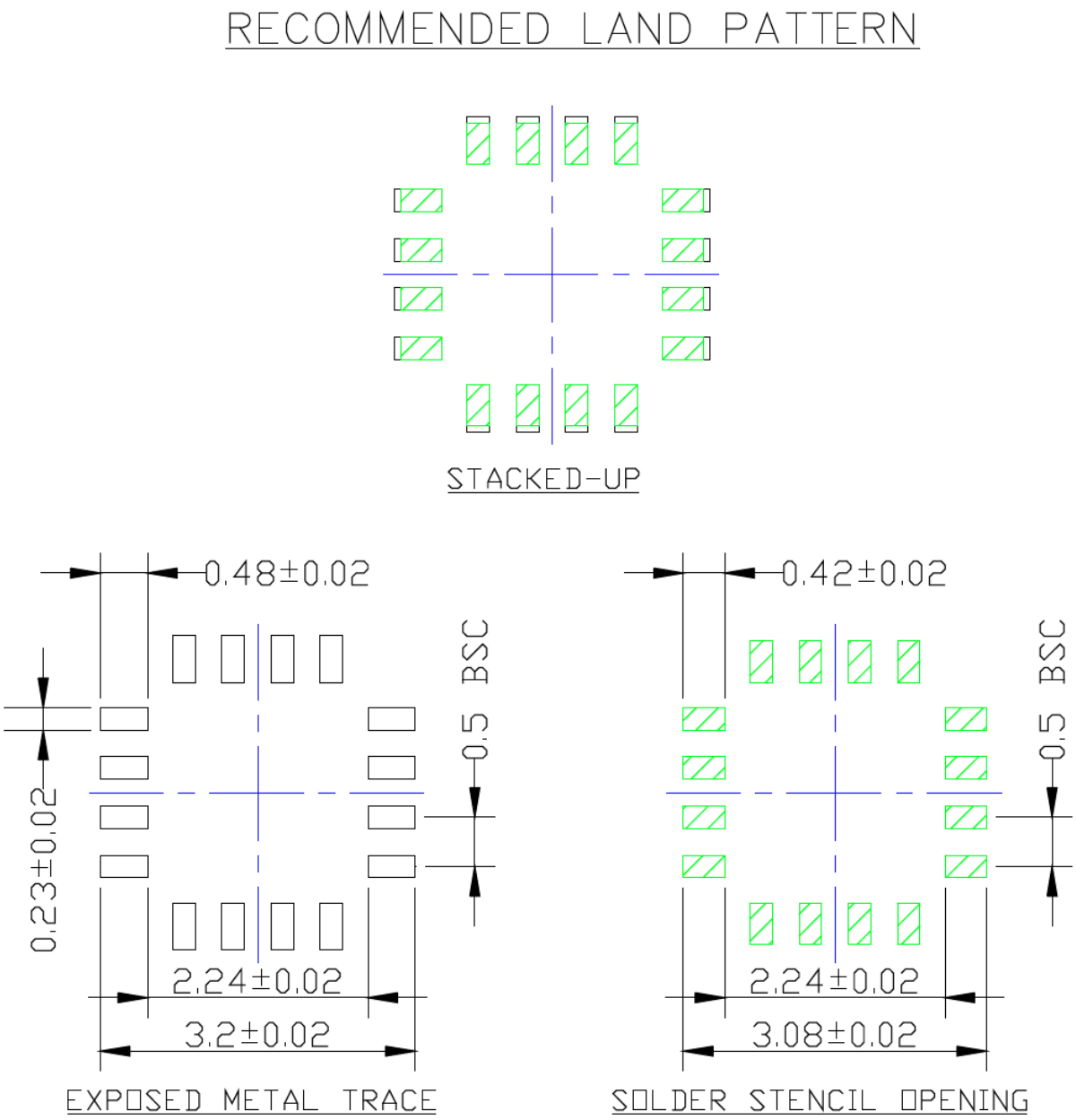
POD-Land Pattern drawing #CQFN33-16LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (November 2017)

- Converted Micrel document MIC2810 to Microchip data sheet DS20005910A.
- Minor text changes throughout.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–	XX	X	X	–	XX[1]
Device		Output Voltages	Temperature	Package		Tape and Reel Option

Device:	MIC2810:	Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs
Output Voltages: (DC/DC, LDO1, LDO2)	1JGM=	1.25V/1.8V/2.8V
	1J6J =	1.25V/1.4V/2.5V
	1J6S =	1.25V/1.4V/3.3V
	44M =	1.2V/1.2V/2.8V
	4GK =	1.2V/1.8V/2.6V
	4GM=	1.2V/1.8V/2.8V
	4GP =	1.2V/1.8V/3.0V
	4GS =	1.2V/1.8V/3.3V
	4LS =	1.2V/2.7V/3.3V
	4MS =	1.2V/2.8V/3.3V
	CGJ =	1.2V/1.8V/2.5V
	FGS =	1.5V/1.8V/3.3V
Temperature:	Y =	Pb-Free with Industrial Temperature Grade (–40°C to +125°C)
Package:	ML =	16-lead, 3 mm x 3 mm QFN, 0.85 mm thickness
Tape and Reel:	TR =	5,000/Reel

Examples:

a) MIC2810-44MYML-TR: Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.2V/1.2V/2.8V Output Voltage, –40°C to +125°C, 16LD QFN Package, 5,000/Reel

b) MIC2810-4GMYML-TR: Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.2V/1.8V/2.8V Output Voltage, –40°C to +125°C 16LD QFN Package, 5,000/Reel

c) MIC2810-4GSYML-TR: Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.2V/1.8V/3.3V Output Voltage, –40°C to +125°C 16LD QFN Package, 5,000/Reel

d) MIC2810-4MSYML-TR: Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.2V/2.8V/3.3V Output Voltage, –40°C to +125°C 16LD QFN Package, 5,000/Reel

e) MIC2810-FGSYML-TR: Digital Power Management IC 2 MHz, 600 mA DC/DC with Dual 300 mA/300 mA Low VIN LDOs, 1.5V/1.8V/3.3V Output Voltage, –40°C to +125°C 16LD QFN Package, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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