
AVR[®] DD Product Brief

Introduction

The AVR[®] DD MCU (AVR DD) family of microcontrollers is using the AVR[®] CPU with hardware multiplier running at clock speeds up to 24 MHz. They include 16/32/64 KB of Flash, 2/4/8 KB of SRAM, and 256 bytes of EEPROM. The microcontrollers are available in 14-, 20-, 28-, 32-pin packages. The family uses the latest technologies from Microchip Technology, with a flexible and low-power architecture, including Event System, intelligent analog features, and advanced digital peripherals.

Features

- AVR[®] CPU
 - Running at up to 24 MHz
 - Single-cycle I/O access
 - Two-level interrupt controller
 - Two-cycle hardware multiplier
 - Supply voltage range: 1.8V to 5.5V
- Memories
 - 16/32/64 KB in-system self-programmable Flash memory
 - 2/4/8 KB SRAM
 - 256B EEPROM
 - 32B of user row in nonvolatile memory that can keep data during chip erase and be programmed while the device is locked
 - Write/erase endurance
 - Flash 10,000 cycles
 - EEPROM 100,000 cycles
 - Data retention: 40 years at 55°C
- System
 - Power-on Reset (POR) circuit
 - Brown-out Detector (BOD)
 - Clock options
 - High-precision internal high-frequency oscillator with selectable frequency up to 24 MHz (OSCHF)
 - Auto-tuning for improved internal oscillator accuracy
 - Internal PLL up to 48 MHz for high-frequency operation of Timer/Counter type D (PLL)
 - 32.768 kHz ultra-low power internal oscillator (OSC32K)
 - 32.768 kHz external crystal oscillator (XOSC32K)
 - External clock input
 - External high-frequency crystal oscillator (XOSCHF) with clock failure detection
 - Single-pin Unified Program and Debug Interface (UPDI)
 - Three sleep modes
 - Idle with all peripherals running for immediate wake-up
 - Standby with a configurable operation of selected peripherals

- Power-Down with full data retention
 - Automated Cyclic Redundancy Check (CRC) Flash memory scan
 - Watchdog Timer (WDT) with Window mode, with a separate on-chip oscillator
 - External interrupt on all general purpose pins
- Peripherals
 - One 16-bit Timer/Counter type A (TCA) with three compare channels for Pulse-Width Modulation (PWM) and waveform generation
 - Up to three 16-bit Timer/Counter type B (TCB) with input capture and signal measurements
 - One 12-bit PWM Timer/Counter type D (TCD) optimized for power control
 - One 16-bit Real-Time Counter (RTC) that can run from external crystal or internal oscillator
 - Up to two USARTs
 - Operation modes: RS-485, LIN slave, master SPI, and IrDA
 - Fractional baud rate generator, auto-baud, and start-of-frame detection
 - One SPI with master/slave operation modes
 - One Two-Wire Interface (TWI) with dual address match
 - Simultaneous master/slave operation (dual mode)
 - Philips Inter-Integrated Circuit (I²C) compatible
 - Standard mode (Sm, 100 kHz)
 - Fast mode (Fm, 400 kHz)
 - Fast mode plus (Fm+, 1 MHz) ⁽¹⁾
 - Event System for CPU independent and predictable inter-peripheral signaling
 - Configurable Custom Logic (CCL) with up to four programmable Look-up Tables (LUTs)
 - One 12-bit differential 100 ksp/s Analog-to-Digital Converter (ADC)
 - One 10-bit Digital-to-Analog Converter (DAC)
 - One Analog Comparator (AC)
 - One Zero-Cross Detector (ZCD)
 - Internal 1.024V, 2.048V, 2.500V and 4.096V voltage references, and external reference option (VREF)
- I/O and Packages:
 - Multi Voltage I/O (MVIO) on I/O port C
 - Up to 27/26 programmable I/O pins
 - 32-pin VQFN 5x5 mm and TQFP 7x7 mm
 - 28-pin SPDIP, SSOP, and SOIC
 - 20-pin SOIC and QFN 4x4 mm
 - 14-pin SOIC
- Temperature Ranges:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C

Note:

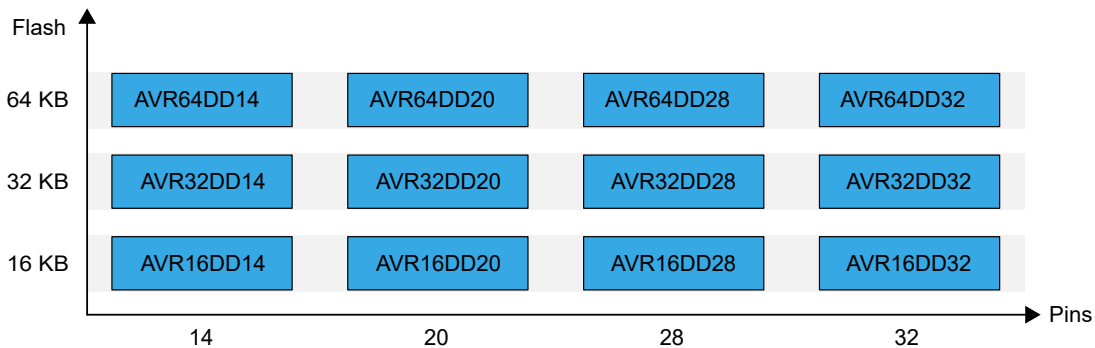
1. I²C Fm+ is only supported for 2.7V and above.

AVR[®] DD Family Overview

The figure below shows the AVR DD devices, laying out pin count variants and memory sizes:

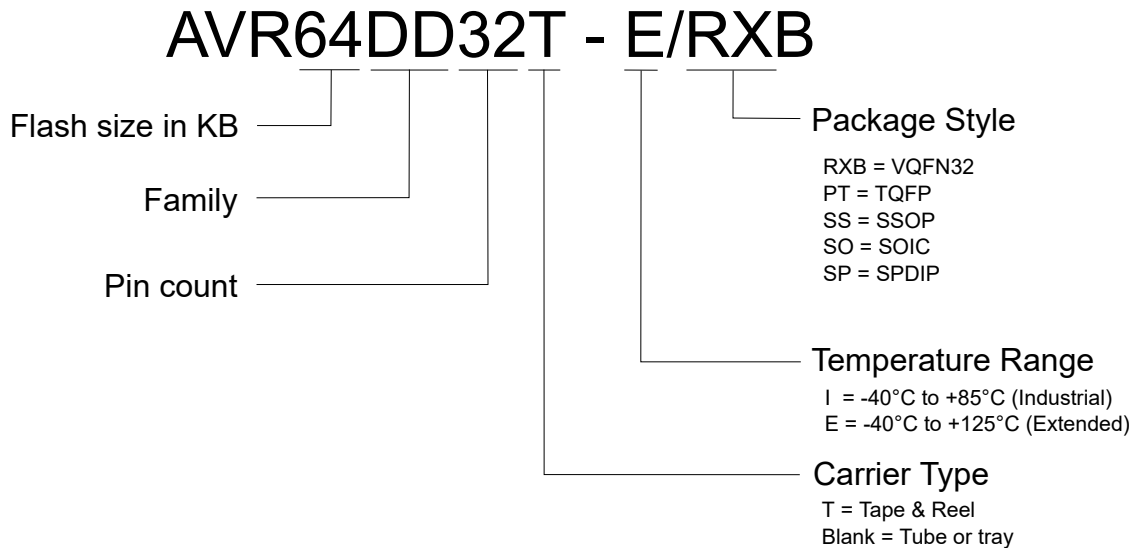
- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1. AVR[®] DD Family Overview



The name of a device in the AVR DD family is decoded as follows:

Figure 2. AVR[®] DD Device Designations



Memory Overview

The following table shows the memory overview of the entire AVR DD family.

Table 1. Memory Overview

Devices	AVR16DD14 AVR16DD20 AVR16DD28 AVR16DD32	AVR32DD14 AVR32DD20 AVR32DD28 AVR32DD32	AVR64DD14 AVR64DD20 AVR64DD28 AVR64DD32
Flash memory	16 KB	32 KB	64 KB
SRAM	2 KB	4 KB	8 KB
EEPROM	256B	256B	256B
User row	32B	32B	32B

Peripheral Overview

The following table shows the peripheral overview of the entire AVR DD family.

Table 2. Peripheral Overview

Feature	AVR16DD14 AVR32DD14 AVR64DD14	AVR16DD20 AVR32DD20 AVR64DD20	AVR16DD28 AVR32DD28 AVR64DD28	AVR16DD32 AVR32DD32 AVR64DD32
Pins	14	20	28	32
Max. frequency (MHz)	24	24	24	24
16-bit Timer/Counter type A (TCA)	1	1	1	1
16-bit Timer/Counter type B (TCB)	2	2	3	3
12-bit Timer/Counter type D (TCD)	1	1	1	1
Real-Time Counter (RTC)	1	1	1	1
USART	2	2	2	2
SPI	1	1	1	1
TWI/I ² C ⁽¹⁾	1 ⁽¹⁾	1 ⁽¹⁾	1 ⁽¹⁾	1 ⁽¹⁾
12-bit differential ADC (channels) ⁽²⁾	1 (7) ⁽²⁾	1 (13) ⁽²⁾	1 (19) ⁽²⁾	1 (23) ⁽²⁾
10-bit DAC (outputs)	1(1)	1(1)	1(1)	1(1)
Analog Comparator (AC)	1	1	1	1
Zero-Cross Detector (ZCD)	1	1	1	1
Peripheral Touch Controller (PTC)	-	-	-	-
Operational amplifier (OP)	-	-	-	-
Configurable Custom Logic Look-up Table (CCL LUT)	4	4	4	4
Watchdog Timer (WDT)	1	1	1	1
Event System (EVSYS) channels	6	6	6	6
General Purpose I/O ⁽³⁾	11/10 ⁽³⁾	17/16 ⁽³⁾	23/22 ⁽³⁾	27/26 ⁽³⁾

.....continued				
Feature	AVR16DD14 AVR32DD14 AVR64DD14	AVR16DD20 AVR32DD20 AVR64DD20	AVR16DD28 AVR32DD28 AVR64DD28	AVR16DD32 AVR32DD32 AVR64DD32
Pins	14	20	28	32
PORT	PA[1:0], PC[3:1], PD[7:4], PF[7:6]	PA[7:0], PC[3:1], PD[7:4], PF[7:6]	PA[7:0], PC[3:0], PD[7:1], PF[7,6,1,0]	PA[7:0], PC[3:0], PD[7:1], PF[7:0]
External interrupts	11	17	23	27
CRCSCAN	1	1	1	1
Unified Program and Debug Interface (UPDI)	1	1	1	1

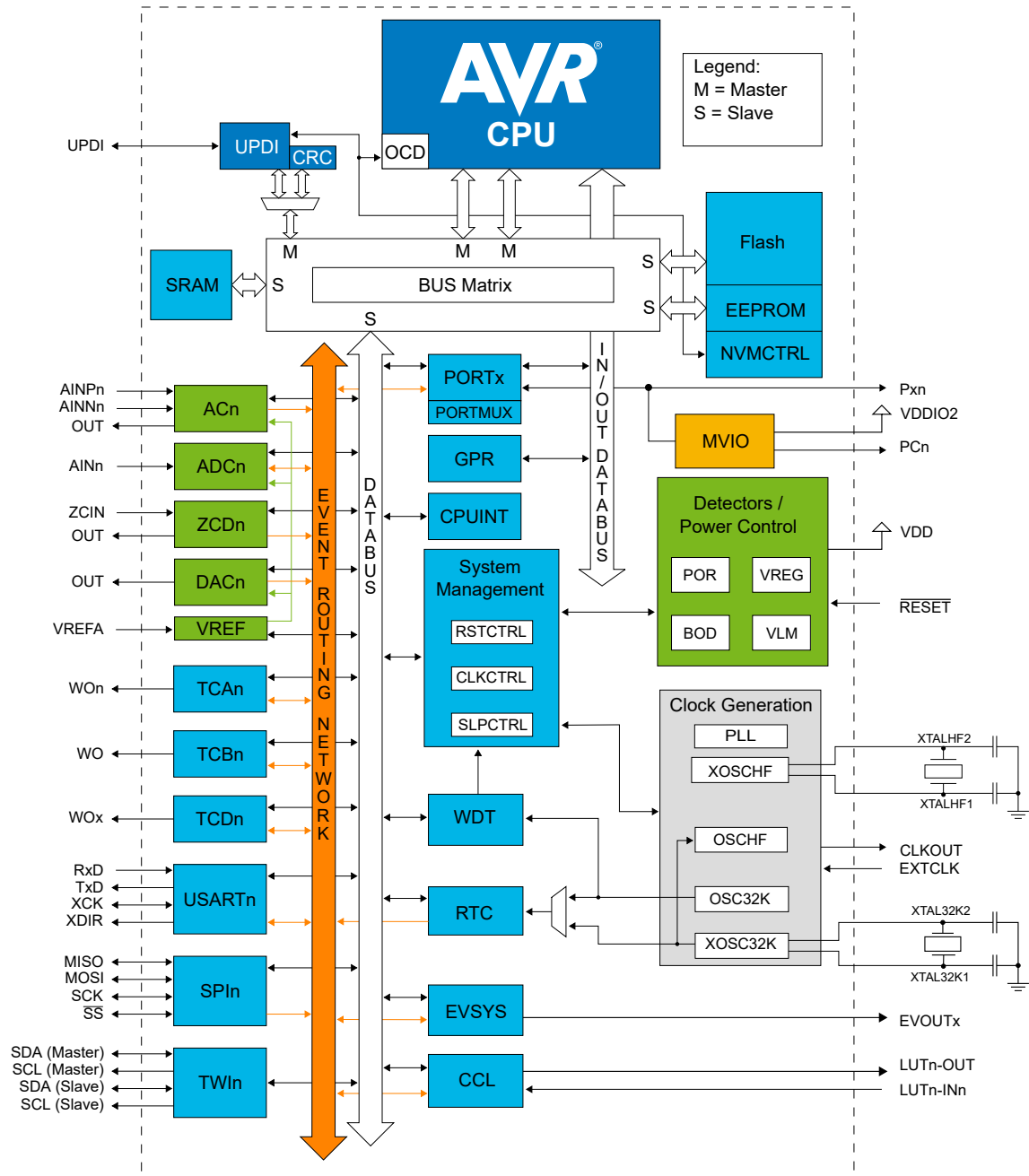
Notes:

1. The TWI/I²C can operate simultaneously as both master and slave on different pins.
2. ADC inputs are available on MVIO pins (PORTC) if the MVIO is disabled in the MVSYSSEN fuse setting.
3. PF6/RESET pin is input only.

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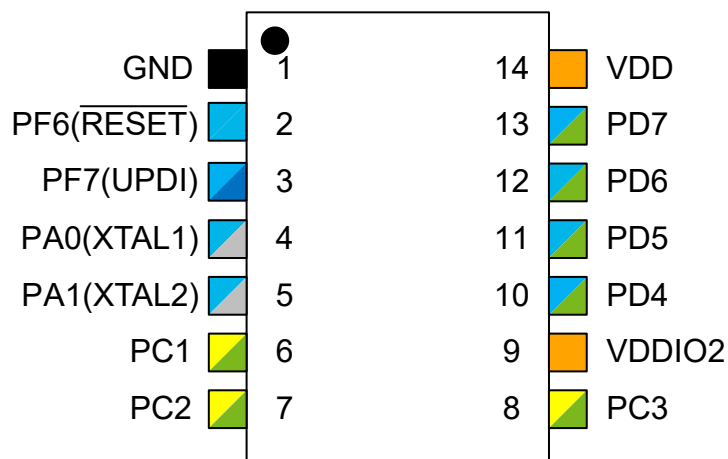
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1. Block Diagram



2. Pinout

2.1 14-Pin SOIC



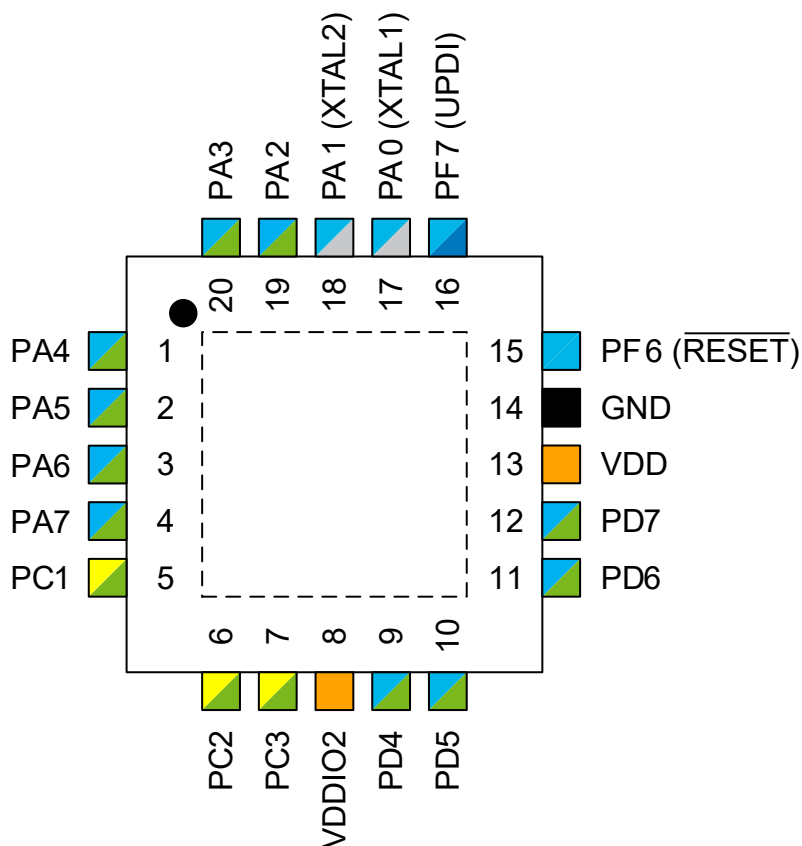
Power

-  Power Supply
-  Ground
-  Pin on VDD Power Domain
-  Pin on VDDIO2 Power Domain

Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function

2.2 20-Pin VQFN



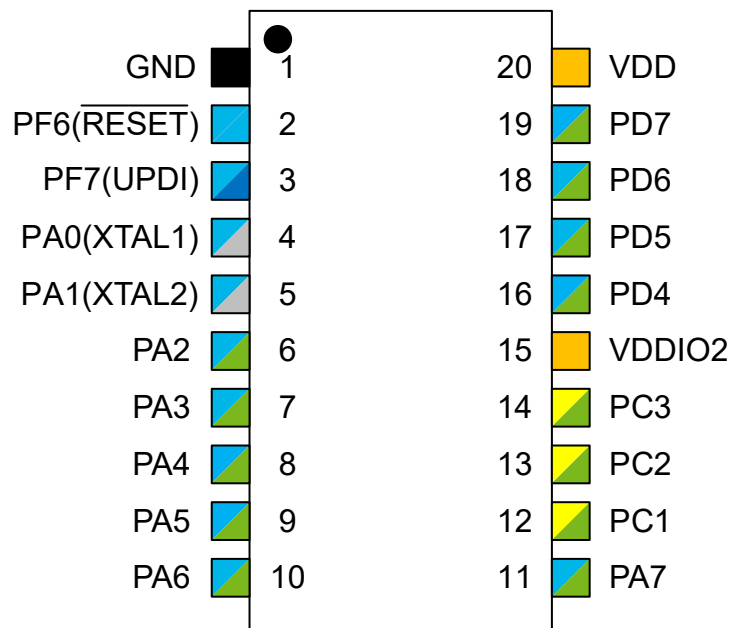
Power

-  Power Supply
-  Ground
-  Pin on VDD Power Domain
-  Pin on VDDIO2 Power Domain

Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function

2.3 20-Pin SOIC



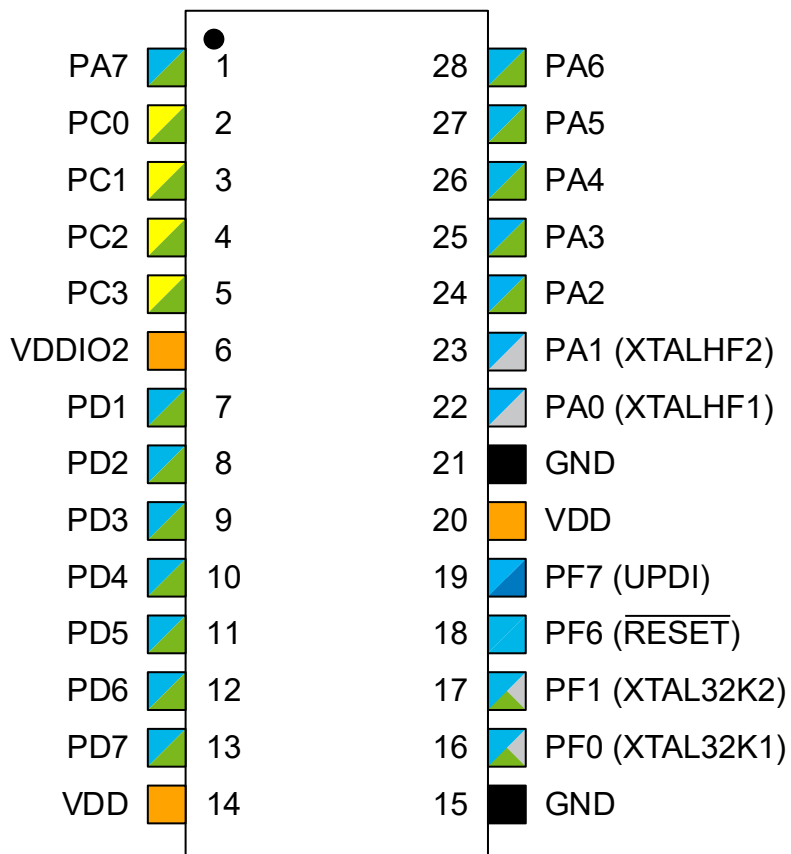
Power

-  Power Supply
-  Ground
-  Pin on VDD Power Domain
-  Pin on VDDIO2 Power Domain

Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function

2.4 28-Pin SPDIP, SSOP and SOIC



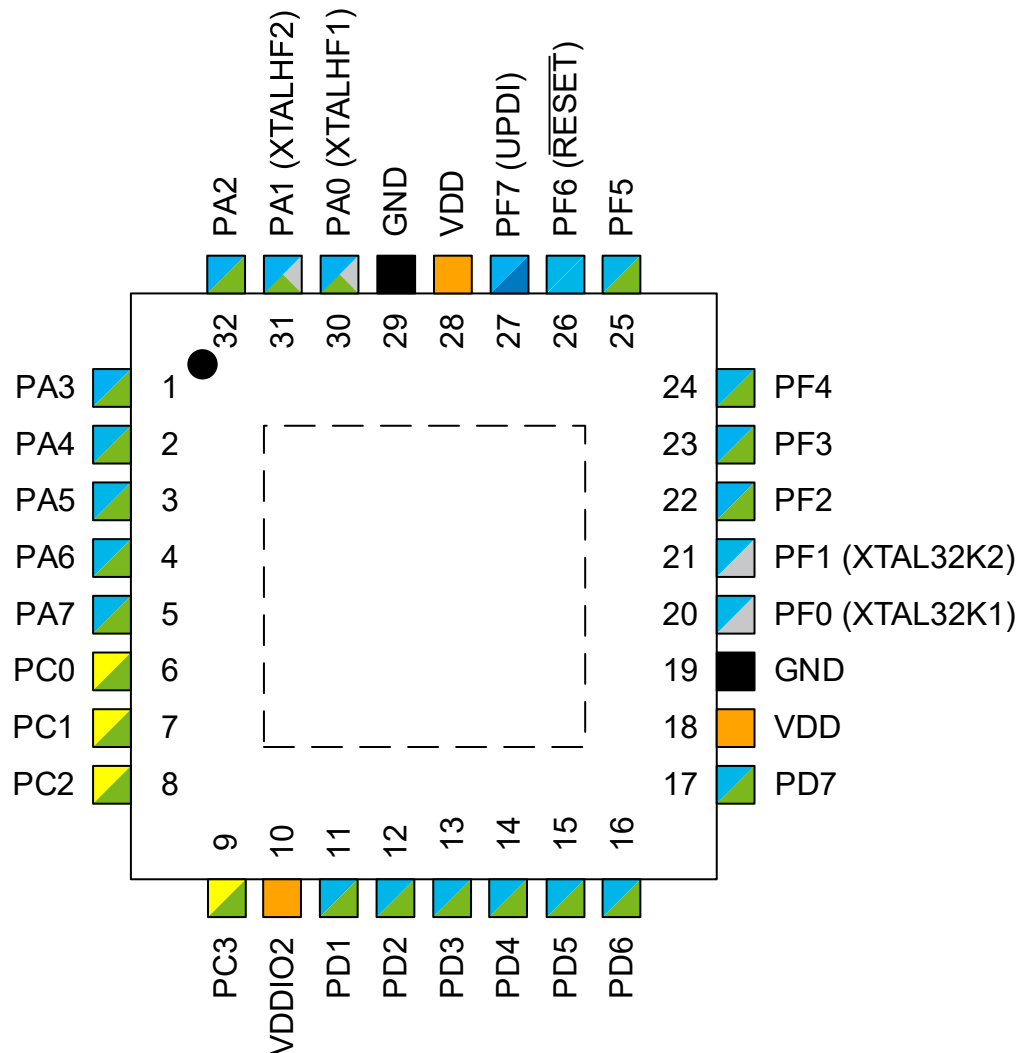
Power

-  Power Supply
-  Ground
-  Pin on VDD Power Domain
-  Pin on VDDIO2 Power Domain

Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function

2.5 32-Pin VQFN and TQFP



Power

 Power Supply

 Ground

 Pin on VDD Power Domain

 Pin on VDDIO2 Power Domain

Functionality

 Programming/Debug

 Clock/Crystal

 Digital Function Only

 Analog Function

3. I/O Multiplexing and Considerations

3.1 I/O Multiplexing

VQFN32 TQFP32	SPDI28 SQC28 SSOP28	VQFN20	SQC20	SQC14	Pin name (1,2)	Special	ADC0	AC0	DAC0	ZCD3	USARTn	SPI0	TW0(4)	TCA0	TCBn	TC00	EVSYS	CCL
30	22	17	4	4	PA0	XTAL32K1 ⁽⁷⁾ XTALHF1 EXTCLK					0,TxD	MOSI ⁽³⁾	SDA(M) ⁽³⁾	WO0				LUT0,IN0
31	23	18	5	5	PA1	XTAL32K2 ⁽⁷⁾ XTALHF2					0,RxD	MISO ⁽³⁾	SCL(M) ⁽³⁾	WO1				LUT0,IN1
32	24	19	6		PA2	TwI Fm+	AIN22				0,XCK 0,TxD ⁽³⁾		SDA(M)	WO2	0,WO		EVOUTA	LUT0,IN2
1	25	20	7		PA3	TwI Fm+	AIN23				0,XDIR 0,RxD ⁽³⁾		SCL(M)	WO3	1,WO			LUT0,OUT
2	26	1	8		PA4		AIN24				0,TxD ⁽³⁾	MOSI		WO4		WOA		
3	27	2	9		PA5		AIN25				0,RxD ⁽³⁾	MISO		WO5		WOB		
4	28	3	10		PA6		AIN26				0,XCK ⁽³⁾	SCK				WOC		LUT0,OUT ⁽³⁾
5	1	4	11		PA7	CLKOUT	AIN27	OUT		ZCOUT	0,XDIR ⁽³⁾	SS				WOD	EVOUTA ⁽³⁾	
6	2				PC0		AIN28 ⁽⁶⁾				1,TxD	SCK ⁽³⁾ MOSI ⁽³⁾		WO0 ⁽³⁾	2,WO			LUT1,IN0
7	3	5	12	6	PC1		AIN29 ⁽⁶⁾				1,RxD 0,TxD ⁽³⁾	SS ⁽³⁾ MISO ⁽³⁾ MOSI ⁽³⁾		WO1 ⁽³⁾				LUT1,IN1
8	4	6	13	7	PC2	TwI Fm+	AIN30 ⁽⁶⁾	AINN3 ⁽⁶⁾		ZCIN	1,XCK 0,RxD ⁽³⁾	SCK ⁽³⁾ MISO ⁽³⁾	SDA(S) SDA(M) ⁽³⁾	WO2 ⁽³⁾			EVOUTC	LUT1,IN2
9	5	7	14	8	PC3	TwI Fm+	AIN31 ⁽⁶⁾	AINP4 ⁽⁶⁾			1,XDIR 0,XCK ⁽³⁾	SS ⁽³⁾ SCK ⁽³⁾	SCL(S) SCL(M) ⁽³⁾	WO3 ⁽³⁾				LUT1,OUT
10	6	8	15	9	VDDIO2													
11	7				PD1		AIN1							WO1 ⁽³⁾				LUT2,IN1
12	8				PD2		AIN2	AINP0						WO2 ⁽³⁾			EVOUTD	LUT2,IN2
13	9				PD3		0,AIN3	AINN0						WO3 ⁽³⁾				LUT2,OUT
14	10	9	16	10	PD4		AIN4				0,TxD ⁽³⁾	MOSI ⁽³⁾		WO4 ⁽³⁾		WOC ⁽³⁾		
15	11	10	17	11	PD5		AIN5				0,RxD ⁽³⁾	MISO ⁽³⁾		WO5 ⁽³⁾		WOD ⁽³⁾		
16	12	11	18	12	PD6		AIN6	AINP3	VOUT		0,XCK ⁽³⁾ 1,TxD ⁽³⁾	SCK ⁽³⁾						LUT2,OUT ⁽³⁾
17	13	12	19	13	PD7	VREFA	AIN7	AINN2			0,XDIR ⁽³⁾ 1,RxD ⁽³⁾	SS ⁽³⁾					EVOUTD ⁽³⁾	
18	14	13	20	14	VDD													
19	15	14	1	1	GND													
20	16				PF0	XTAL32K1	AIN16							WO0 ⁽³⁾		WOA ⁽³⁾		LUT3,IN0
21	17				PF1	XTAL32K2	AIN17							WO1 ⁽³⁾		WOB ⁽³⁾		LUT3,IN1
22					PF2	TwI Fm+	AIN18							WO2 ⁽³⁾		WOC ⁽³⁾	EVOUTF	LUT3,IN2
23					PF3	TwI Fm+	AIN19							WO3 ⁽³⁾		WOD ⁽³⁾		LUT3,OUT
24					PF4		AIN20							WO4 ⁽³⁾	0,WO ⁽³⁾			
25					PF5		AIN21							WO5 ⁽³⁾	1,WO ⁽³⁾			
26	18	15	2	2	PF6 ⁽⁵⁾	RESET												
27	19	16	3	3	PF7	UPDI						SS ⁽³⁾					EVOUTF ⁽³⁾	

AVR® DD Family

I/O Multiplexing and Considerations

.....continued

VQFN32 TQFP32	SPDIP28 SOIC28 SSOP28	VQFN20	SOIC20	SOIC14	Pin name (1,2)	Special	ADC0	AC0	DAC0	ZCD3	USARTn	SPI0	TWI0(4)	TCA0	TGBn	TCD0	EVSYS	CCL
28	20				VDD													
29	21				GND													

Notes:

1. The pin names are of Pxn type, with x being the PORT instance (A, B, C, ...) and n, the pin number. The notation for signals is PORTx_PINn. All pins can be used as event input.
2. All pins can be used for external interrupt.
3. Alternate pin positions. For selecting the alternate positions, refer to PORTMUX - Port Multiplexer section.
4. The TWI pins that can be used as master or slave are marked *M*. The pins with slave-only are marked *S*.
5. Input-only.
6. ADC and AC inputs are available on MVIO pins (PORTC) if the MVIO is disabled in the MVSYSSEN fuse setting.
7. Only for 14-pin and 20-pin devices.

4. Data Sheet Revision History

Note: The data sheet revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc. Rev.	Date	Description
A	06/2020	Initial document revision

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