S32G2PB

S32G2 Product Brief

High-performance vehicle network processor based on Arm® Cortex®-M7 and Cortex-A53 technology

Rev. 8.1 — April 2021

Product Brief

Contents

1 Applications

The S32G2 chip family targets the following applications:

- Central gateways and domain controllers connecting various networks and translating their protocols
- Safety processor for ADAS and autonomous driving
- High-performance central compute nodes
- FOTA masters controlling secure software image downloads and their distribution to the ECUs in the network
- Secure key management
- Smart antennas

2 Block diagram

The following figure shows the block diagram for S32G274A, the superset chip in the S32G2 family.

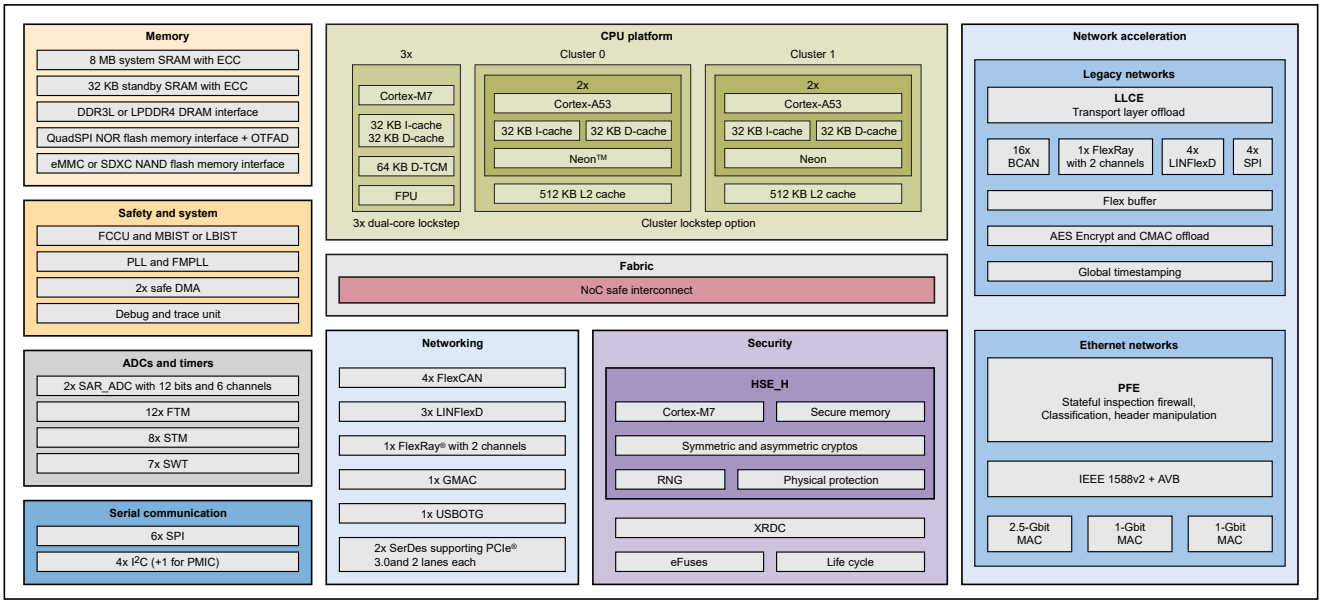

Figure 1. Block diagram

3 Feature comparison

The following table compares the features of chips in the S32G2 family.

Table 1. Feature comparison

Feature	S32G234M	S32G233A	S32G254A	S32G274A
Compute and bus modules				
CPUs: applications	N/A	Cluster 0: single Cortex-A53 core (only core 0 is available on these chips)		Cluster 0: dual Cortex-A53 core
		Cluster 1: single Cortex-A53 core (only Core 0 is available on these chips)		Cluster 1: dual Cortex-A53 core
L1 cache	N/A	32 KB I-cache and 32 KB D-cache per Cortex-A53 core		
L2 cache	N/A	512 KB per cluster		
Cache coherency interconnect	N/A	Yes		
Interrupt controller for Cortex-A53 core	N/A	Generic interrupt controller (CoreLink™ GIC-500)		
Core maximum frequencies	Cortex-M7 core: 400 MHz	Cortex-A53 core: 1 GHz Cortex-M7 core: 400 MHz		
Lockstep support for Cortex-A53 cores	N/A	Configurable: lockstep clusters or two independent clusters		
CPUs: real-time	3 Cortex-M7 cores in lockstep	1 Cortex-M7 core in lockstep (only the Cortex-M7 core 0 is avaialable on these chips)	3 Cortex-M7 cores in lockstep	
L1 cache	32 KB I-cache and 32 KB D-cache per Cortex-M7 core			
DTCM	64 KB per Cortex-M7 core			
Interrupt controller for Cortex-M7 core	3 NVICs	1 NVIC	3 NVICs	
DMA	2 eDMA (supporting lockstep), each with 32 channels			
DMAMUX inputs	128 per DMA			
Debug run control	Arm CoreSight™ JTAG (IEEE 1149.1)			
Debug trace	Aurora 4-lane			
SWT	7			
STM	8			
Memory modules				
System RAM	8 MB	6 MB	8 MB	
System RAM ports	16 ports, interleaved 64-byte			
DRAM	N/A	LPDDR4 and DDR3L		
DRAM physical interface (PHY)	N/A	×32		

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Table 1. Feature comparison (continued)

Feature	S32G234M	S32G233A	S32G254A	S32G274A
QuadSPI	1 (supports two identical devices)			
uSDHC	1			
Fuses	8 KB bank			
Standby SRAM with ECC	32 KB			
Security modules				
Security subsystem	HSE_H			
Resource isolation	XRDC supporting 8 domains			
Arm TrustZone®	N/A	Yes		
Life cycle	Yes			
Secure debug	Yes			
OTFAD	Yes			
Communication interface modules				
Comms acceleration	LLCE			
CAN with flexible data rate	16 (in LLCE) + 4			
FlexRay with dual-channel support for protocol version 2.1	1 (in LLCE) + 1			
LINFlexD	4 (in LLCE) + 3			
SPI	4 (in LLCE, can be enabled with firmware) + 6			
Ethernet acceleration	PFE			
MAC	4 (3 PFE_MAC + 1 GMAC_0)			
Supported Ethernet interfaces	MII, RMII, RGMII, and SGMII			
SerDes subsystem with PCIe	1 supporting Gen2 in X1 and X2 modes (PCIe_1 only)	2 supporting Gen3 in X1 and X2 modes		
SerDes subsystem lanes	2 configurable for PCIe or SGMII (SerDes_1 only)	4 configurable for PCIe or SGMII		
USBOTG	N/A	1 supporting USB 2.0 and ULPI interfaces		
I^2C	5			
CRC	1			
Generic modules				
PIT	2			
SAR_ADC	2, each supporting 12 bits and 6 channels			

Table continues on the next page...

Table 1. Feature comparison (continued)

Feature	S32G234M	S32G233A	S32G254A	S32G274A
FTM	2, each supporting 6 channels			
CTU	1			
SEMA42	1			
Clocking, power, and reset				
FIRC frequency	48 MHz			
SIRC frequency	32 kHz			
FXOSC frequency	20–40 MHz			
PLL	5			
Low-power mode	Yes			
RTC	1 with API function			
Wake-up sources	24			
Miscellaneous				
Package	525 flip chip plastic ball grid array (525 FC-PBGA), 19 mm × 19 mm, 0.8 mm pitch			

4 Process technology and power design

The S32G2 chip family is based on the following process technology and general power design concepts:

- Fabricated in 16nm FinFET (16FFC) process technology
- Low-power design
  - Dynamic clock gating of cores and peripherals
  - Standby power-gated mode allowing wake-up (with 32 KB retained RAM) from a subset of input pins, a timer, or both
  - Software-controlled clock gating of peripherals

5 Operating parameters

The operating parameters for the S32G2 family are as follows:

- 0.8 V ± 5% for digital core input supply voltage
- 1.1–3.45 V digital input-output rail (pad segments supporting 1.8 V and 3.3 V)
- 1.71–1.95 V digital input-output rail for PCIe
- 1.1 V or 1.35 V DDR pads for LPDDR4 or DDR3L and a 1.8 V supply
- 1.71–1.95 V for analog-to-digital converter reference and analog input pins
- Selectable output edge rate control (slow, medium, or fast)
- Designed with EMI reduction techniques
  - Phase-locked loop
  - Core and system clock with frequency modulation
  - On-chip bypass capacitance
  - Software-selectable output edge rate control

  - Schmitt trigger on selected inputs
- Configurable pins
  - Selectable pullup, pulldown or no pull on all SIUL2-controlled pins
  - Selectable open drain
- Nonpredefined pins configurable as GPIO
- Compatible with NXP VR5510 PMIC

6 Operating conditions and environmental constraints

The following table describes the operating conditions and environmental constraints under which chips in the S32G2 family are fully operational.

Table 2. Operating conditions and environmental constraints

Parameter	Condition or constraint
Fully static operation	Up to 1 GHz max frequency modulation (Cortex-A53 core clock)
Digital I/O input supply voltages	
For pad segments supporting 1.8 V and 3.3 V nominal supply voltage	1.68–1.92 V and 3.08–3.52 V
For pad segments supporting only 1.8 V nominal supply voltage	1.68–1.92 V (minimum tolerance)
Digital core input supply voltage	0.75–0.87 V or 0.72–0.87 V
Analog-to-digital converter reference[1] and analog input pins	1.71–1.95 V
Junction temperature	–40 °C to +125 °C
Particle radiation	
Alpha particle flux[2]	< 0.001 alpha/cm^2/h
High-energy cosmic neutron flux	< 14 neutrons/cm^2/h (from 10 to 800 MeV)[3]
Mission profile	
Lifetime with 10% operating time and chip powered off when not operating	10 years (equivalent to 8760 hours of active operation)
Weighted junction temperature over lifetime	105 °C
Electrostatic discharge (ESD)	250 V CDM AEC Q100-011 level C3 2 kV HBM AEC Q100-002 level H2

1. Reference pins supply both converter reference and internal switch.
2. Low alpha mold compound material (if applicable) and low bump flux required.
3. Following the JESD-89 standard (normal background neutron flux at sea level in New York, NY)

7 Module features

7.1 Compute and bus modules

7.1.1 Cortex-A53 core complex

- Up to 1 GHz Arm Cortex-A53 MPCore with four processors in two MP2 clusters and a Snoop Control Unit (SCU) that you can use to ensure coherency within the cluster. The two clusters are connected with a cache-coherent interconnect.
- Optionally configurable lockstep capability between clusters (second cluster in lockstep with first cluster)
- Implements Armv8 AArch64 and AArch32 ISA
- AArch64 execution state:
  - Contains thirty-one 64-bit general purpose registers, with a 64-bit program counter, stack pointer, and exception link registers.
  - Provides a single instruction set, A64.
  - Defines the Armv8 exception model, with four exception levels, EL0–EL3, that provide an execution privilege hierarchy.
  - Includes virtual addresses (VAs) held in 64-bit registers. The Cortex-A53 core's VMSA implementation maps these to 40-bit physical address (PA) maps.
  - Defines a number of PSTATE elements that hold processor state. The A64 instruction set includes instructions that operate directly on various PSTATE elements.
  - Names each system register using a suffix that indicates the lowest exception level at which you can access the register.
- AArch32 execution state:
  - Is backwards-compatible with implementations of the Armv7-A architecture profile that include the security and virtualization extensions.
  - Contains thirteen 32-bit general purpose registers, a 32-bit program counter, stack pointer, and link register. Some of these registers have multiple banked instances for use in different processor modes.
  - Provides two instruction sets, A32 and T32.
  - Provides an exception model that maps the Armv7 exception model onto the Armv8 exception model and exception levels. For exceptions taken to an exception level that is using AArch32, this supports the Armv7 exception model use of processor modes.
  - Features 32-bit VAs. The VMSA maps these to PA maps that can support PAs of up to 40 bits.
  - Collects processor state into the current processor state register.
- L1 instruction and data caches, each 32 KB in size
- 512 KB L2 cache for each cluster
- Eight-stage pipeline
- 2.8–3.2 DMIPS/MHz (depending on compiler options)
- Private Timer per core
- Cortex-A53 Neon Media Processing Engine coprocessor
- Vector floating-point version 3 (VFPv3) architecture extension for floating-point computation that is fully compliant with the IEEE 754 standard
- The Cortex-A53 core implements the Arm generic interrupt controller with GICv4 architecture profile.
- One 128-bit AXI master interface per cluster
- Parity or ECC protection for the SRAMs (the L1 and L2 caches and other memories) within the cluster

7.1.2 GIC-500

GIC-500 works together with the Cortex-A53 cluster to handle interrupts. It implements the Arm Generic Interrupt Controller Architecture Specification version 3.0 to enable support for Armv8 cores.

With the following software-configurable settings of the GIC-500, interrupts can be:

- Enabled or disabled.
- Assigned to one of two groups, Group 0 or Group 1.
- Prioritized.
- Signaled to different processors in multiprocessor implementations.
- Level-sensitive or edge-triggered.

GIC-500 implements:

- GIC security extensions that support:
  - Group 0 interrupts as secure interrupts
  - Group 1 interrupts as nonsecure interrupts
- GIC virtualization extensions that provide hardware support for managing virtualized interrupts
- The following interrupt types:
  - 16 software-generated interrupts
  - Private peripheral interrupts for each processor
  - A configurable number of shared peripheral interrupts
  - Message-based interrupts that you generate by writing to the AXI4 slave port
  - An interrupt translation service that provides ID translation and core migration for message-based interrupts

7.1.3 Cache coherency interconnect (CCI)

CCI maintains the coherency of the Cortex-A53 clusters, with non-CPU master accesses to system resources. It supports:

- Cortex-A53 CPUs as fully-coherent initiators
- SerDes and GMAC as input-output coherent initiators

7.1.4 Cortex-M7 core complex

The main features of the Cortex-M7 core complex include:

- Operating frequency up to 400 MHz
- In-order issue, super-scalar pipeline with dynamic branch prediction
- DSP extensions
- FPU
- The Armv7-M Thumb® instruction set, defined in the Armv7-M Architecture Reference Manual
- Two-way set-associative L1 instruction and data caches (32KB each) with parity error and ECC protection
- 64 KB of DTCM split equally between lower and upper TCM
- Backdoor system bus port that provides TCM access to other bus masters
- Configurable NVIC
- Memory protection unit with 16 regions
- Advanced configurable debug and trace components

- Embedded trace macrocell
- Low-power features including architectural clock gating, sleep mode and wake-up interrupt controller
- Delayed lockstep operation with output comparison for ISO 26262

7.1.5 NVIC

NVIC supports and manages low latency interrupt processing. It includes registers for managing interrupt sources, interrupt behavior, and interrupt routing to the Cortex-M7 core. It allows you to:

- Enable, disable, and generate processor interrupts from peripheral interrupt sources.
- Generate software interrupts.
- Mask and prioritize interrupts.

7.1.6 eDMA

eDMA is a third-generation module that performs complex data movements via 32 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes the following to minimize the overall block size:

- A DMA engine that performs source address calculations, destination address calculations, and the actual data-movement operations
- An SRAM-based memory containing the TCDs for the channels.

eDMA has the following features:

- 32 channels that support independent 8-, 16-, or 32-bit single-value or block transfers
- Variable-sized queues and circular queues
- Independent configuration of source and destination address registers to post-increment or remain constant
- A peripheral, CPU, or eDMA channel request initiates each transfer
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories and peripheral registers such as serial interfaces, analog-to-digital converters, timers, and so on
- Works with DMAMUX so you can assign any DMA source to any available DMA channel (see DMAMUX)
- Software-based abort operation
- Buffer memory with ECC protection and fault insertion
- Built-in CRC generation for transferred data
- Virtualization support (channel programming model organized in 4 KB pages per channel)

In delayed lockstep configuration, RCCUs:

- Compare the operation of two identical eDMA modules.
- Report any discrepancies to FCCU for an appropriate system reaction to the fault.

See RCCU and FCCU for more details.

7.1.7 DMAMUX

This chip has two DMAMUX instances per eDMA pair with different trigger inputs. Each instance has the following features:

- Independently-selectable DMA channel routers (inputs) for each DMA peripheral slot:
  - 8 periodic DMA triggers from PIT (4× PIT_0, 4× PIT_1)
  - Total of 32 DMA slots (DMAMUX output)

- Each channel router is assigned to one of the following sources:
  - One of the peripheral DMA sources
  - The always-enabled source

7.1.8 Debug

The debug system supports the following:

- CoreSight debug infrastructure
- JTAG (IEEE 1149.1) with up to five pins:
  - TDI
  - TDO
  - TMS
  - TCK
  - JCOMP{TRST}
- Debug of all computing engines, including accelerators (access via APB interface), with breakpoints and run control
- Security-related features:
  - A range of security levels from no JTAG to fully-open based on eFuse configuration for both debug and test
  - Secured and nonsecured invasive and non-invasive debug to allow further granularity in debug accesses
  - Support for field return parts to open access for debug and test to allow failure analysis
- Debug capabilities:
  - Access to core and memory-mapped resource examination and modification
  - Monitor mode
  - Halt mode
  - Breakpoint and watchpoint control, with the Cortex-A53 core supporting six breakpoints and four watchpoints
- System profiling and performance monitoring
- Trace capabilities:
  - Instruction trace of all Cortex-A53 CPUs
  - Instrumentation trace of all Cortex-A53 CPUs
  - Instruction trace of all Cortex-M7 CPUs
  - Instruction trace of sequence CPUs
  - Data trace of AHB peripherals
  - Data trace of AHB bus masters
  - Data trace of external DRAM traffic (with address filtering)
  - Data trace of internal SRAM traffic (with address filtering)
  - Single- and multi-core trace generation
  - Global time stamping
- Arm Real Time trace Interfaces: Aurora Trace Port
  - For Aurora trace port: 4× lanes with up to 2.5 GHz
  - 40 MHz target maximum frequency

- Trace to internal memory
- Cross trigger
- Watchpoints in the SRAMC and DDR controller data path:
  - Comparators to monitor address and master ID
  - Pairing of comparators to create address and master ID ranges
  - Configurable for any or all of these accesses:
    - Read
    - Write
    - Execute
  - Breakpoint generation for watchpoint hits

7.1.9 SWT

SWT offers the following features:

- 32-bit timeout register to set the timeout period
- Timer running on 48 MHz internal RC-oscillator clock for increased functional safety
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt after an initial timeout
- Master access protection
- Hard- and soft-configuration lock bits
- Reset configuration inputs allow you to enable the timer out of reset

7.1.10 STM

STM offers these features:

- 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in Debug mode

7.2 Memory modules

7.2.1 SRAMC

SRAMC interfaces between the bus system and the system RAM arrays. The chip contains 16 SRAMCs interleaved across the full SRAM block.

The SRAMCs offer the following features:

- 640 KB RAM array per SRAMC, for a total of 8 MB
- Interleaved on 64-byte boundaries, aligned to 128-bit wide cache line access
- 128-bit data, nonblocking, interface to system interconnect, supporting multiple outstanding transactions
- ECC support on 64-bit boundaries

7.2.2 DDR subsystem

The DDR subsystem on this chip contains one 32-bit-wide DDR memory controller to connect to off-chip DDR memories.

The DDR subsystem offers the following features:

- LPDDR4 and DDR3L
- 16-bit and 32-bit DRAM memories, allowing up to two ranks
- One or two DRAM devices to be connected per DDRCTRL in parallel
- Clock frequency of up to 1600 MHz (3200 MHz double data rate) on the DDR memory interface for LPDDR4
- Clock frequency of up to 800 MHz (1600 MHz double data rate) on the DDR memory interface for DDR3L
- Up to 32 bits of addressable memory space
- Scheduler and reordering queue to optimize transaction order for reads and writes to improve utilization (out of order execution of reads)
- Quality of service features to accelerate critical transactions
- Inline ECC scheme to protect the data stored in DRAM (single error correct, double error detect), optimized to reduce bandwidth impact
- Region support for the inline ECC with seven configurable regions

7.2.3 QuadSPI

QuadSPI is an interface for external quad serial flash memories for code storage, data storage, and code execution. It offers the following features:

- Industry-standard single, dual, quad, octal mode serial flash memories
- 1.8 V interface only
- DDR serial flash memory for high performance
- Operating modes:
  - 1 × 4-bit
  - 1 × 1-bit with up to 80 MHz clock in DDR mode and 108 MHz in SDR mode
- Octal I/O serial flash memory with data strobe support: 1 × 8-bit
- Octal I/O in DDR mode with 200 MHz clock and 8-bit data
- Octal I/O in SDR mode up to 133 MHz clock and 8-bit data
- Differential clock support for 1.8 V HyperFlash devices
- Access to external flash memory such that the resulting peak read bandwidth is 400 Mbytes/s
- Execute in Place (XiP)
- Flexible buffering scheme with multi-master prioritized access
- On-the-fly decryption of the data in the external flash memory (AES-128) to enable security (OTFAD):
  - Usage of plaintext cipher-based chaining mode for AES to ensure flash-memory integrity
  - Two-dimensional parity support to correct faults
- Single-pass decryption and authentication for security purposes
- Fault detection to improve fault robustness
- Programmable sequence engine
  - Enables future command or protocol changes

  - Supports all existing vendor commands and operations
  - Requires you to select the corresponding sequence according to the connected flash-memory device
- OTFAD engine that implements only AES CTR mode with an authentication scheme that:
  - Allows single-pass encryption or authentication
  - Validates the absence of a fault
- Parity on the flash-memory interface

7.2.4 uSDHC

uSDHC offers the following features:

- Conforms to the SD Host Controller Standard Specification version 3.1
- Compatible with:
  - MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0/5.1
  - SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
  - SDIO Card Specification version 3.0
- Designed to work with these cards:
  - SD
  - miniSD
  - SDIO
  - miniSDIO
  - SD Combo
  - MMC
  - MMC-plus
  - RS-MMC cards
- Card bus clock frequency up to 200 MHz, HS200/HS400/HS400 Enhanced Strobe
- 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes
  - SDIO cards using 4 parallel data lines
    - In SDR mode: Up to 832 Mbps of data transfer
    - In DDR mode: Up to 400 Mbps of data transfer
  - SDXC cards using 4 parallel data lines
    - In SDR mode: Up to 832 Mbps of data transfer
    - In DDR mode: Up to 400 Mbps of data transfer
  - MMC cards using 8 parallel data lines
    - In SDR mode: Up to 1600 Mbps of data transfer
    - In DDR mode: Up to 3200 Mbps of data transfer
- Single block and multi-block read and write
- Block sizes of 1–4096 bytes
- Write protection switch for write operations
- Synchronous and asynchronous abort

- Pause during the data transfer at block gap
- SDIO Read Wait and Suspend Resume operations
- Auto CMD12 for multi-block transfer
- Host can initiate nondata transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes
- Interrupt period
- Fully-configurable 256×32-bit FIFO for reading and writing data
- Internal and external DMA capabilities
- Voltage selection by configuring vendor-specific register field
- Advanced DMA to perform linked memory access

7.3 Security and boot modules

7.3.1 HSE_H

HSE_H is a subsystem that implements the security functions for the chip. It provides cryptographic services to host CPUs and the network accelerators, targeting current security specifications (for example, SHE, HSM, and EVITA Full). HSE_H establishes the root of trust on the chip during the boot process.

HSE_H provides the following features:

- Secure boot of customer code using asymmetric or symmetric keys
- Highly-featured symmetric and asymmetric accelerators
- In-hardware cryptographic functions:
  - AES (up to 256)
  - SHA-1
  - SHA-2
  - Wide support of elliptic curves (ECC)
  - RSA (up to 4096)
- TRNG
- PRNG
- Protection against various tamper and side-channel attacks
- Glitch attack countermeasures
- FOTA support

7.3.2 XRDC

XRDC provides an integrated, scalable architectural framework for access control, system memory protection and peripheral isolation. It allows you to assign chip resources including processor cores, noncore bus masters, memory regions and slave peripherals to processing domains to support enforcement of robust operational environments. This occurs in the following sequence:

1. Each bus mastering resource is assigned to a domain identifier (domain ID).
2. The access control policies for the individual domains are programmed into any number of slave memory region descriptors and slave peripheral domain access control registers.

3. All accesses throughout the device are monitored concurrently to determine the validity of each and every access. If a reference from a given domain has sufficient access rights, it is allowed to continue. Otherwise, the access is aborted and error information captured.

XRDC defines an access-control scheme that supports a four-level model, combining the traditional privileged (also known as supervisor) and user modes with an additional signal defining the secure and nonsecure attributes of each memory reference. The result is a four-level hierarchical access control mechanism, where:

SecurePriv(ileged) > SecureUser > NonsecurePriv(ileged) > Non-secureUser

with different access control policies based on read and write references. Combined with the user/privileged and secure/nonsecure attributes, a domain ID is associated with every system bus transaction and forms the hardware basis for implementation of XRDC's access control mechanisms.

You can control access to shared memory regions and slave peripherals dynamically with a hardware semaphore. If you enable a hardware semaphore for a given address space or peripheral, then writes to the targeted address space are only allowed if the requesting domain owns the semaphore. This capability allows the access control policy for a given resource to be dynamically revised based on semaphore ownership.

XRDC's key features include:

- Assignment of chip resources to processing domains. Resources are categorized into 4 groups:
  - Processor cores
  - Noncore bus masters
  - Slave memories
  - Slave peripherals

  Each domain is assigned a unique domain ID. This domain ID is a new attribute associated with every system bus transaction. The domain ID is also used in conjunction with user, privileged, secure, and nonsecure attributes.
- Access rights to slave targets defined in region descriptor registers for memories
- Access control registers for peripherals
- Sharing of memory and peripherals with inclusion of hardware semaphores to dynamically determine access rights
- Built upon a 4-level hierarchical access control model
  - SecurePriv(ileged) > SecureUser > NonsecurePriv(ileged) > Non-secureUser
  - Encoded into a 3-bit per-domain access control policy used throughout XRDC
  - Certain processors do not support the Non-securePriv level. For these cores, the model simplifies to a 3-level definition: SecurePriv > SecureUser > NonsecureUser

7.3.3 Arm TrustZone technology

The Arm TrustZone security extensions are supported in the Cortex-A53 processors. The TrustZone signals from the processors are used within XRDC to maintain resource isolation at a system level. At a processor level, the Arm TrustZone software stack is compatible to elevate between secure and nonsecure privilege states. At a system level, XRDC configures system resource isolation.

7.3.4 Life cycle

The chip supports a life-cycle mechanism that progressively increases security through product development and production. This mechanism controls level of protection for key access, boot configuration, and debug.

These are the supported life cycle states:

- Customer Deliverable
- OEM Production

- In Field
- Failure Analysis

Life cycle states can only progress forward to the next sequential state.

7.3.5 Boot assist ROM (BAR)

BAR is the default location from which the chip always starts the boot process. The boot process depends on the reset type, boot configuration pins and eFuses.

BAR offers the following features:

- Read the image vector table and boot data structures
- Optionally download image to memory
- Allow download and decryption of AES-encrypted images from external flash memory
- Retrieve Device Configuration Data (DCD) from the external program image
- Alternate serial boot-loading via FlexCAN or LINFlexD
- Supports network boots via Ethernet using TFTP
- Execute image
- Initiate download of the HSE_H firmware
- Secure boot

The execution of the BAR code starts from HSE_H.

You can configure the execution of your application code to start on either the Cortex-M7 or Cortex-A53 processor.

7.4 Clocking, power, and reset

7.4.1 FIRC

FIRC offers these features:

- 48 MHz nominal frequency
- Inverter-based comparator that does not require a current source
- ± 5% variation over voltage and temperature after process trim
- If PLL detects a loss of lock or loss of clock, the FIRC clock output serves as the system clock source
- Serves as the default system clock during startup

7.4.2 SIRC

The chip includes a 32 kHz SIRC for low-power (standby) operation.

7.4.3 FXOSC

FXOSC offers these features:

- Crystal Input mode
- Oscillator input frequency of 20 MHz, 24 MHz, or 40 MHz
- PLL reference
- Bypass capability

7.4.4 PLLs

The chip has several PLLs:

- One Arm PLL for CPUs and high-speed chip interconnects supporting frequency modulation (programmable)
- One DDR PLL for the DRAM interface
- One PERIPH PLL for peripherals including FlexCAN and FlexRay (not frequency modulated)
- One AURORA PLL for the Aurora debug interface
- One ACCEL PLL for PFE
- Two PCIE PLLs for the PCIe interfaces

The PLLs have the following major features:

- Modes of operation:
  - Bypass
  - Normal PLL with crystal reference (default)
  - Normal PLL with external reference
  - Normal PLL with internal RC oscillator input (for example, for operation during boot)
- Lock monitor circuitry with lock status
- Loss-of-lock detection
- Option to switch on and off the frequency modulation
- DFS outputs for additional fractionally-divided clock domains

7.4.5 Power management

The power management architecture includes the following:

- Interface to an external PMIC that provides all the device voltages
- Supply presence detectors for all power segments
- Power modes:
  - Run
  - Standby
- Standby mode functionality:
  - 23 external wake-up sources
  - Real-time clock, using internal 32 kHz SIRC
  - Autonomous periodic interrupt supporting wake-up
  - 32 KB retained RAM
- Hardware control of Run mode entry
- Software control of Standby mode entry, and wake-up event management for Standby exit
- Software control of subsystem disabling to reduce power consumption during Run mode

7.4.6 RTC

The chip contains one RTC with API functionality that can perform 32-bit comparisons. It offers these features:

- Interrupt generation
- Wake-up from Standby mode

- 32-bit counter that supports times up to greater than 1.5 months with 1 ms resolution
- Selectable clock source from:
  - SIRC
  - FIRC
  - External pin
- Optional 512 prescalers and optional 32 prescalers connected in series in the clock path feeding the 32-bit counter
- 32-bit compare value to support interrupt intervals of 1 second up to greater than 1 hour with 1 second resolution
  - 32-bit compare value to support wake-up intervals of 1.0 ms to 1 s
  - Wake-up logic has separate enable to support changing compare value while RTC runs
  - Operates in all chip modes of operation

7.4.7 WKPU

WKPU offers these features:

- Nonmaskable interrupt support with:
  - One external NMI pin
  - Glitch filter
  - Active (rise or fall) edge selection control for events
- External wake-up and interrupt support with:
  - 23 external wake-up or interrupt pins
  - Individual glitch filters
  - Independent interrupt mask
  - Individual active (rise or fall) edge selection control for events
  - Configurable system wake-up triggering from all interrupt sources
  - Individual wake-up boot mode selection
  - Individual pin pullup and pulldown enable control

7.5 Safety modules

7.5.1 RCCU

RCCU checks all outputs (addresses, data, and control signals) of the delayed-lockstep blocks. It offers the following features:

- Guarantees the highest-possible diagnostic coverage (check of checker)
- Used as checkers for:
  - eDMA
  - Cortex-M7 core output signals
  - Cortex-A53 core output signals
- Redundancy of the checks by replicated compare units for the ECC encoded signal groups

7.5.2 FCCU

FCCU provides an independent fault-reporting mechanism even in case the CPU is misbehaving.

FCCU offers the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the chip
- Collection of test results
- Register that reports the chip status
- You can select critical signals from different fault sources inside the chip
- Configurable and graded fault control
  - Internal reactions that you can program
    - No reaction
    - Latched into a register
    - Alarm interrupt or NMI
    - Full-chip reset request to MC_RGM
  - External reaction
    - Two configurable output pins report a failure to the outside world
    - Disabling of a set of communication controllers (for example FlexRay, CAN, and GMAC)
- FCCU output supervision unit
- 5 fault inputs that you can directly trigger

7.5.3 Thermal Monitoring Unit (TMU)

TMU is a temperature sensor that supports functional safety by performing high-temperature checks. It offers the following features:

- Ambient temperature range from -40 °C to +105 °C
- Accuracy at temperatures +111°C to 125 °C is ±3 °C
- Accuracy at temperatures equal to or below +110 °C is ± 8 °C or better
- Output is readable via digital interface or alternatively measured via the on-chip ADC to provide digital code corresponding to temperature
- Calibration table for TMU trimming
- Multiple sites to sense temperature

7.5.4 Built In Self-Test modules (BIST)

This chip includes the following protection against latent faults:

- Software triggered self-test of volatile memory (SRAM) and read-only memory (test pattern written and checked by MBIST) and random logic (scan-chain based test pattern generated and checked by LBIST)

7.5.5 Safety by Software (SBSW)

SBSW has the following features:

- 64 TMC instances
- Each TMC implements a comparator where the comparison event is observed by TMC time monitor for proper timing behavior
- Interface for TMWDP with 64 automata; TMWDP models and observes the correct logical and temporal sequence of application events

- TMWDP timer for driving TMWDP clock period
- A controller that:
  - Aggregates TMWDP and TMC statuses
  - Controls the access to TMC and TMWDP configuration registers
  - Drives the fault reporting to FCCU

7.6 Communication interface modules

7.6.1 LLCE

LLCE is a dedicated subsystem optimized to manage CAN, LIN, and FlexRay communications. LLCE includes the following functionality:

- 16 BCAN channels
- 4 LINFlexD channels
- 2 FlexRay channels (A+B)
- 4 LPSPI hardware interfaces can be enabled with LLCE firmware

LLCE is a firmware-based architecture. The standard NXP LLCE firmware offers the following features:

- Transmission lookup hardware acceleration
- Reception lookup hardware acceleration
- An efficient fire-and-forget interface for the host interface, which reduces the load on the host CPU by enabling a nonblocking interface
- Time synchronization across all interfaces, which enables a common time base across all networks
- Full implementation of these specifications:
  - Classic CAN and CAN FD protocol specification, version ISO 11898-1:2015
  - FlexRay Communications System Protocol specification, version 2.1 Rev A
  - LIN protocol specification, version 1.3, 2.0, 2.1 and 2.2

Because LLCE is a firmware-based solution, you can potentially develop advanced features:

- Data-consistency checking
- Data formatting
- Diagnostic mirroring
- Local routing tables
- Intrusion-detection software
- Security offload using HSE_H to secure all CAN, LIN, and FlexRay frames
- Enabling security services at the lowest possible layer
- SPI expansion ports to add additional interfaces (for example, SPI-to-QuadLIN)

A subset of the BCAN, FlexRay, and LINFlexD modules are implemented outside of LLCE (see Feature comparison). These are implemented on the main peripheral bus and do not fully use all LLCE features. The following diagram shows this.

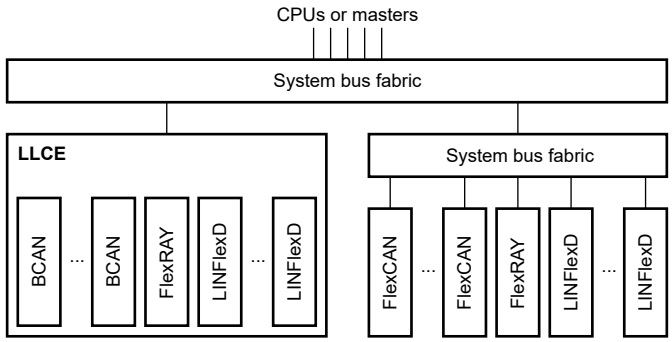


Figure 2. Subset of FlexCAN, FlexRay, and LINFlexD outside LLCE

7.6.2 PFE

The chip uses PFE to provide high-performance Ethernet interfaces.

All ports support MII/RMII and RGMII at 10/100 and 100/1G, respectively. SGMII is supported on three ports at 100M/1G/2.5G, 100M/1G, and 100M/1G.

PFE offers the following features:

- IEEE 802.3 protocol for 10/100/1000/2500 Mbps (rates depend on the PHY interface mode)
- Supports packet sizes from 64 bytes up to 1522 bytes
- L2/3/4 packet classification and header modification—for example,NAT
- Autonomous handling of all packets belonging to a given stream, without host CPU intervention, after stream creation
- Addressing DDR and internal SRAM
- Closely coupled interaction with security coprocessor for IPSec offload
- Routing or bridging an aggregate of 2 Gbps of traffic at minimum packet sizes
- Ingress QoS
- TSN time synchronization (802.1AS-Rev)
- Firmware-based architecture

PFE does not support one of the four S32G Ethernet interfaces. This Ethernet interface, GMAC_0, additionally supports TSN time aware shaping (802.1Qbv) and preemption (802.1Qbu).

The following figure shows the available interfaces.

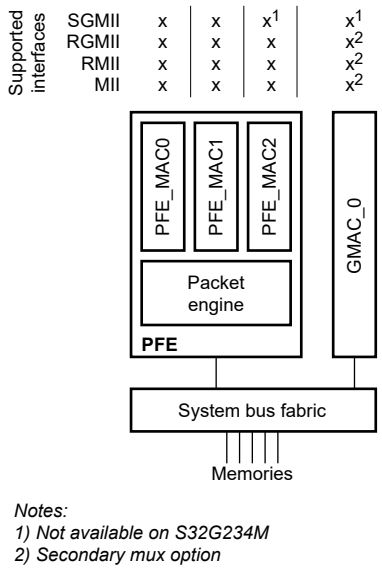


Figure 3. Ethernet interfaces

7.6.3 SerDes subsystem

The S32G2 chips, except S32G234M, contain two SerDes subsystems that include a dual-mode PCI Express Gen3 controller with integrated PHY. S32G234M has only one such subsystem.

Each SerDes subsystem offers these features:

- PCI Express root complex and endpoint modes
- Implementation of the PCI Express 3.0 specification; backwards-compatible with PCIe 2.1 (5 Gbps) and PCIe 1.1 (2.5 Gbps)
- Two-lane configuration for up to 8 Gbps per lane
  - 16 Gbps total
  - 1.97 Gbytes/s net bandwidth after 128/130 bit encoding/decoding
- Transaction layer, link layer and physical layer
- Integrated PHY including transmitter, receiver, PLL, digital core, and ESD
- Maximum payload size of 256 bytes per packet
- AXI bridge module that supports the following features:
  - AXI master and slave interfaces for inbound and outbound PCI Express requests
  - Multifunction support (up to 8 functions) in EP mode
  - All types of PCI Express transactions supported through the AXI bridge
  - A shared AXI slave interface to access the native core's CDM registers
  - Programmable buffer sizes for AXI master and slave requests
  - Programmable MSI interrupt controller to detect and terminate inbound MSI TLP's in the bridge for root complex and dual mode
- Internal DMA support to offload CPU
- Common clock mode with an external reference clock generation for Gen3 and as option an internal reference clock generation for speeds up to Gen2

- Each PHY lane can be optionally used for PFE's SGMII mode, as shown in the following figure

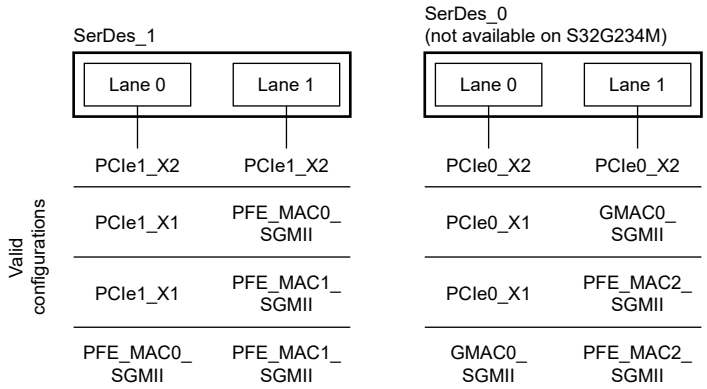


Figure 4. Possible SerDes lane configurations

7.6.4 USBOTG

USBOTG has a ULPI interface and provides point-to-point connectivity. The chip supports an external USB 2.0 PHY using the ULPI interface.

USBOTG offers the following features:

- Complies with USB specification, Rev. 2.0
- Supports High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5Mbps) modes
- USB Host/Device mode (OTG - dual role)
- Suspend and Low-Power modes of operation
- Connects to external PHY using an ULPI interface

7.6.5 I^2C

- Compatible with I^2C 2.0 standard with the exception that HS (high speed) mode is not supported
- Multi-master operation
- Programmable for one of 256 different serial clock frequencies
- Programmable slave address and glitch input filter
- Selectable acknowledge bit
- Interrupt-driven byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation and detection
- Repeated-start signal generation
- Acknowledge bit generation and detection
- Bus-busy detection
- DMA support

7.6.6 SPI

SPI provides a synchronous serial interface for communication between the chip and external devices such as sensors.

SPI offers these features:

- Full-duplex, three-wire synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Extended mode for 32-bit SPI frames
- Up to five chip-select lines, depending on package and pin multiplexing
- Six clock and transfer attributes registers
- Chip-select strobe available as an alternate function on one of the chip-select pins for de-glitching
- FIFOs for buffering as many as five transfers on the transmit and receive side
- Queueing operation possible with eDMA
- Transmit and receive FIFOs can be disabled individually for low-latency updates to SPI queues
- Visibility into transmit and receive FIFOs for ease of debugging
- Programmable transfer attributes on a per-frame basis
- Modified SPI transfer formats for communication with slower peripheral devices

7.6.7 CRC

CRC is a configurable multiple-data-flow unit to compute a cyclic redundancy check on data written to an input register.

CRC offers the following features:

- Three sets of registers to allow three concurrent contexts with possibly different cyclic redundancy check computations, each with different polynomial and seed
- Computes 8-bit, 16-bit or 32-bit wide cyclic redundancy check on the fly (single-cycle computation) and stores result in an internal register
- Implementation of the following standard cyclic redundancy check polynomials:
  - $x^8+x^4+x^3+x^2+1$ (for bits CRC7:CRC0 as defined in VDA CAN protocol according to SAEJ1850). Bits 28:29 of the CRC_CFG register for each context shall be used to select the polynomial preserving compatibility with previous versions of this IP.
  - $x^{16} + x^{12} + x^5 + 1$ (16-bit CRC-CCITT)
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ (32-bit CRC-Ethernet(32))
  - $x^5 + x^3 + x^2 + x + 1$ (CRC-8-H2F AUTOSAR polynomial)
- Key engine to be coupled with communication periphery where cyclic redundancy check application is added to allow implementation of safe communication protocol
- Offloads core from cycle consuming cyclic redundancy check and helps checking configuration signature for safe startup or periodic procedures
- Connected as peripheral bus on IP bus
- DMA

7.7 Generic modules

7.7.1 PIT

This chip has two PITs, PIT_0 and PIT_1. Each PIT offers these features:

- Eight general-purpose interrupt timers
- 32-bit counter resolution and a chaining mode to implement a 64-bit timer
- Uses a 133 MHz clock source
- Channels 0–3 can be used as a trigger for a DMA request

7.7.2 SAR_ADC

Each SAR_ADC offers these features:

- Linear successive approximation algorithm with up to 12-bit resolution at 1.8 V
- Up to 0.5 MS/s sampling rate
- Up to six single-ended external analog inputs, plus additional inputs coming from internal sources
- Single or continuous conversion
- Single-ended 12-bit
- Configurable sample time and conversion speed
- Conversion complete flag and interrupt
- Power Down mode (SAR_ADC in inactive state)
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for various programmable values
- Temperature sensor connected to one channel
- Monitoring of internal supply voltages
- Self-calibration mode and self-test capabilities (supply and capacitive self-test)
- Software-selectable presampling
- 4 analog watchdogs comparing SAR_ADC results against predefined levels (low, high, range) before results are stored in the appropriate SAR_ADC result location
- Programmable DMA enable for each channel

7.7.3 FTM

FTM offers these features:

- Selectable source clock
  - Choose from peripheral PLL, FIRC, or external pin
  - Selecting external clock connects the FTM clock to a chip-level input pin, allowing you to synchronize the FTM counter with an off-chip clock source
- Prescaler divide-by factors of 1, 2, 4, 8, 16, 32, 64, or 128
- 16-bit counter
- 6 channels
  - Each channel can be configured for input capture, output compare, or edge-aligned PWM mode
  - All channels can be configured for center-aligned PWM mode

  - Each pair of channels can be combined to generate a PWM signal with independent control of both edges of PWM signal
  - The FTM channels can operate as pairs with equal outputs, pairs with complementary outputs, or independent channels with independent outputs
  - The polarity of each channel is configurable
  - The generation of an interrupt per channel
- Dead time insertion available for each complementary pair
- Interrupt generation when the counter overflows
- Testing of input captures for a stuck-at-zero and stuck-at-one conditions
- Dual-edge capture for pulse and period width measurements
- Quadrature decoder with input filter, relative position counting and interrupt on position count or capture of position count on external event (channel 0 and 1)
- Trigger input signal from Ethernet IEEE 1588 module

7.7.4 CTU

CTU allows automatic generation of SAR_ADC conversion requests when conditions that you specify occur. The generation occurs without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

CTU offers the following features:

- Cross-triggering between SAR_ADC and FlexPWM
- Double-buffered trigger generation unit with:
  - Up to 8 independent triggers generated from external triggers
  - Operation in Sequential or Triggered modes, based on your configuration
- Trigger delay unit to compensate for the delay of an external low-pass filter
- Double-buffered global trigger unit that allows eTimer synchronization, ADC command generation, or both
- Double-buffered ADC command list pointers to minimize SAR_ADC trigger unit update
- Double-buffered ADC conversion command list with up to 24 ADC commands
- Each trigger can generate consecutive commands
- SAR_ADC conversion command allows to control SAR_ADC channel from each SAR_ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

7.7.5 SEMA42

SEMA42 is a memory-mapped module that provides:

- Robust hardware support needed in multicore systems for implementing semaphores
- A simple mechanism to achieve lock-and-unlock operations via a single write access
- Hardware-enforced gates
- Other useful system functions related to the gating mechanisms

SEMA42 supports 16 hardware-enforced gates in a multiprocessor configuration. Gates appear as a 16-entry byte-size array with read and write accesses. Each hardware gate appears as a 16-state, 4-bit state machine. SEMA42 uses the logical bus master number as a reference attribute, together with the specified data patterns, to validate all write operations. After a gate is locked, it can and must be unlocked by a write of zeroes from the locking processor.

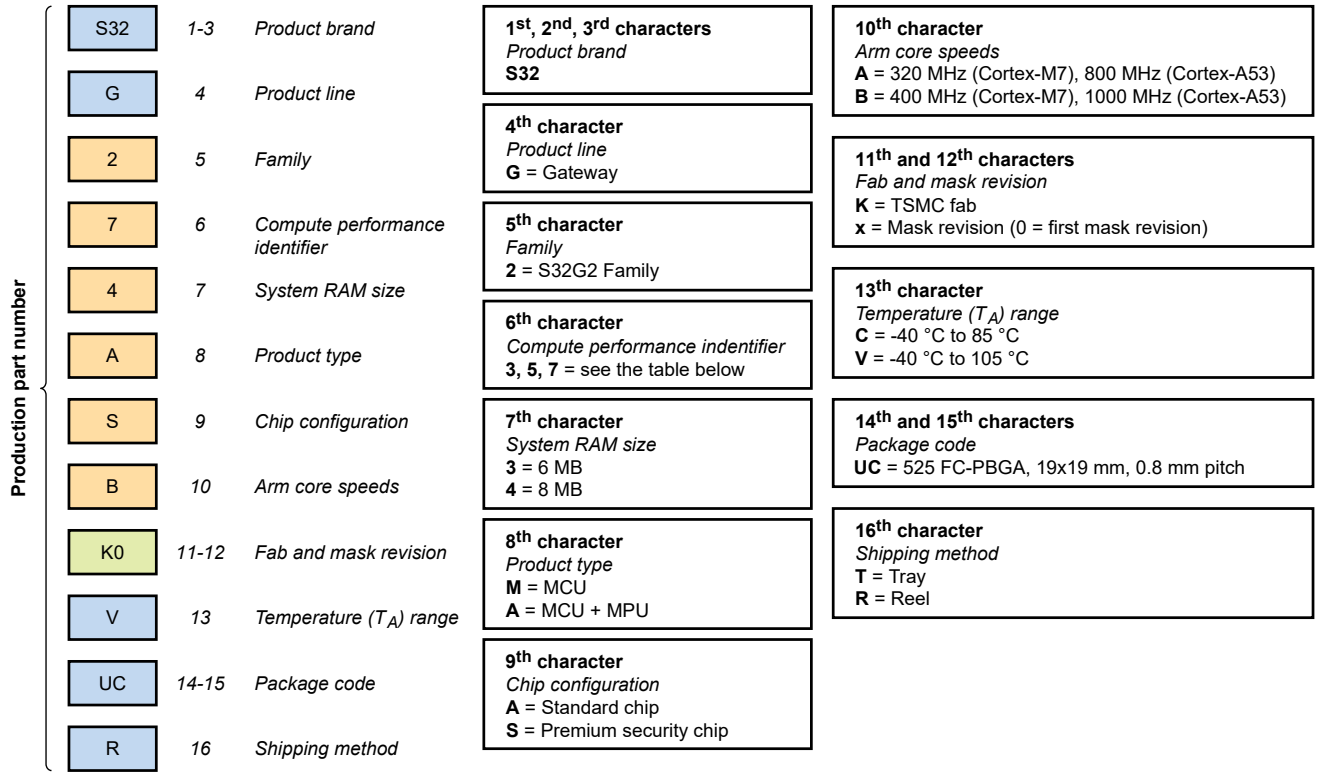
SEMA42 also includes secure reset mechanisms to clear the contents of both individual gates and all gates.

8 Packaging

This chip is available in a 525 FC-PBGA package with the following characteristics:

- 525 balls
- Mechanical dimensions 19 mm × 19 mm, 0.8 mm pitch
- 23 × 23 array with corner balls depopulated

9 Ordering information



	S32G234M	S32G233A	S32G254A	S32G274A
Arm Cortex-M7 cores	3	1	3	3
Arm Cortex-A53 cores	-	2	2	4
System RAM size (MB)	8	6	8	8

Figure 5. Ordering information

10 Glossary

ADAS	Advanced driver-assistance systems
API	Autonomous periodic interrupt
BAR	Boot assist ROM

BCAN	Basic CAN module; part of the LLCE subsystem
CCI	Cache coherency interconnect
CRC	Cyclic Redundancy Check module
CTU	Cross-Triggering Unit module
DDR	Double data rate
DFS	Digital fractional synthesis
DMA	Direct memory access
DMAMUX	Direct Memory Access Multiplexer module
DRAM	Dynamic random-access memory
DTCM	Data tightly-coupled memory
ECC	Error correction code
ECU	Engine control unit
eDMA	Enhanced Direct Memory Access module
FCCU	Fault Collection and Control Unit module
FIRC	Fast Internal RC Oscillator module
FOTA	Firmware over-the-air
FPU	Floating-point unit
FTM	FlexTimer module
FXOSC	Fast External Crystal Oscillator module
GMAC	Gigabit Ethernet Media Access Controller module
HSE_H	Hardware Security Engine subsystem
I^2C	Inter-Integrated Circuit module
LLCE	Low Latency Communication Engine subsystem
NVIC	Nested vectored interrupt controller
OTFAD	On-the-Fly AES Decryption module
PCIe	PCI Express
PFE	Packet Forwarding Engine module
PIT	Periodic Interrupt Timer module
PLL	Phase-locked loop
PRNG	Pseudo random number generator
QuadSPI	Quad Serial Peripheral Interface module
RCCU	Redundancy Control and Checker Unit module
RTC	Real Time Clock module
SAR_ADC	Analog-to-Digital Converter module
SBSW	Safety by Software module
SDR	Single data rate

SEMA42	Semaphores2 module
SIRC	Slow Internal RC Oscillator module
SPI	Serial Peripheral Interface module
SRAMC	SRAM Controller module
STM	System Timer Module
SWT	Software Watchdog Timer module
TCD	Transfer control descriptor
TCM	Tightly-coupled memory
TMC	Time-monitored comparator; part of SBSW
TMU	Thermal Monitoring Unit module
TMWDP	Timed multi-watchdog processor; part of SBSW
TRNG	True random number generator
USBOTG	Universal Serial Bus On-The-Go Controller module
uSDHC	Ultra Secured Digital Host Controller module
WKPU	Wakeup Unit module
XRDC	Extended Resource Domain Controller module

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