Introduction

This application note describes the requirements for a differential interface being referenced to the VIH (Input High Voltage) of an input signal.

Advantages of a Differential Interface

- It offers a wide range of input signaling standards and works with a wide range of input offset voltage.
- Greater immunity to common mode noise. Has tolerance to ground offsets or noise.
- Suitability for use with a low voltage application.
- Less power and substrate noise during signal transition. Current switching much less than single ended interface.
- Reduced EMI due to the cancellation in differential traces.

Requirements of Differential Interface

The input requirement for a differential interface is different from the requirement for a single ended interface. In a single ended interface such as LVCMOS, LVTTL, single-ended HSTL or single-ended PECL/ECL, the V_{OH} and V_{OL} must meet the V_{IH} and V_{IL} requirements of the receivers. In the differential interface, such as LVPECL, HSTL, HCSL, CML, LVDS, or SSTL, the V_{IH} and V_{IL} are no longer referenced. The input parameters VPP and VCMR are now the requirements. Only V_{SWING} and the V_{OH} of the incoming signal are required to meet both V_{PP} and V_{CMR}.

$V_{PP} < V_{SWING} < V_{PP\_MAX}$

$V_{CMR\_MIN} < V_{OH} < V_{CMR\_MAX}$

V_{PP} = Input peak-to-peak voltage requirement

V_{CMR} = Input Common Mode Range Voltage requirement

V_{SWING} = Driver output swing

V_{OH} = Driver output logic high

Figure 1 shows the relationship between V_{SWING}, V_{OH} and V_{PP}, V_{CMR}. The following conditions must be met for a valid input signal: V_{SWING} must be within the required range of the specified V_{PP} and the V_{OH} must be within the V_{CMR} range.

Figure 1. Relationship between Interface Parameters

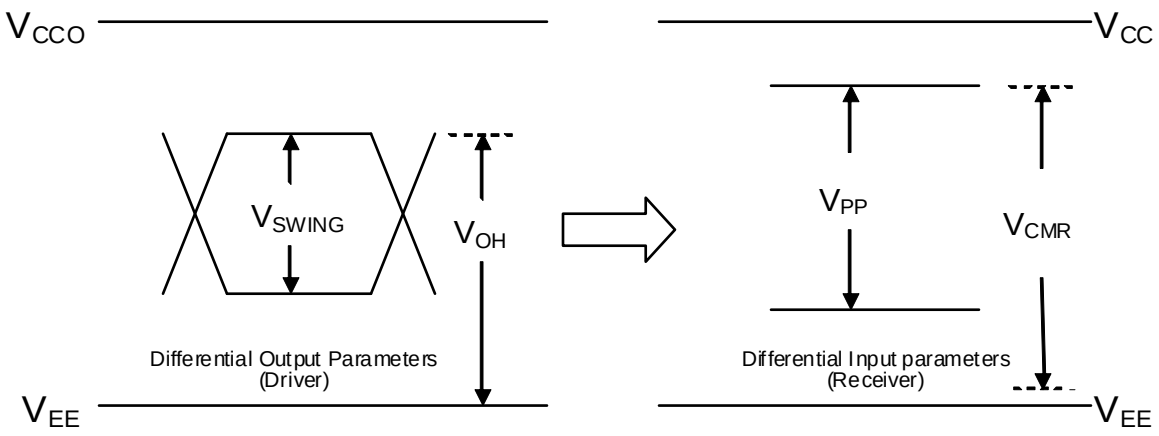


Figure 2. Typical Datasheet for VCMR and VPP

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{PP}	Peak-to-Peak Input Voltage	0.15		1.3	V
V_{CMR}	Common Mode Input Voltage	V_{EE} + 0.5		V_{CC} - 0.85	V

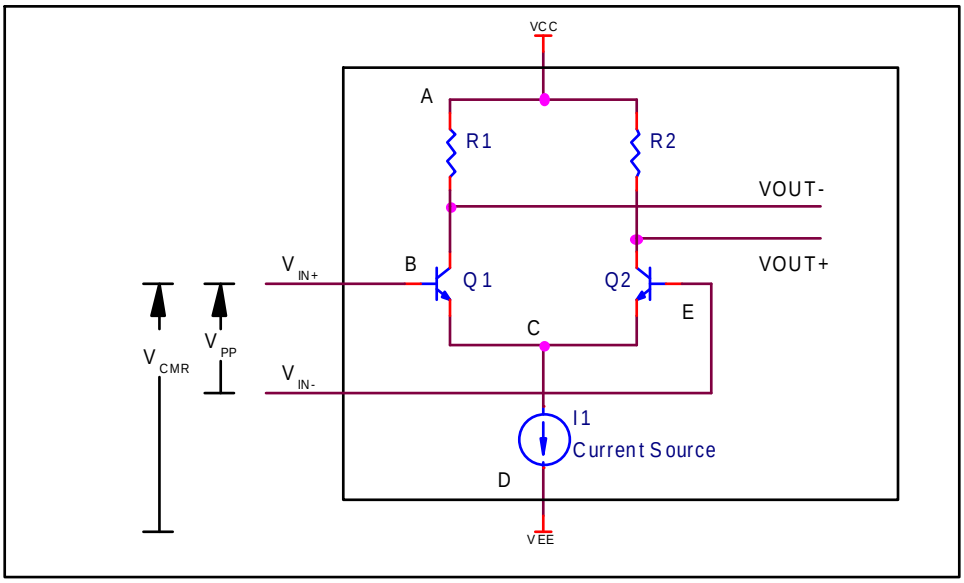
Example

Figure 2 shows a typical datasheet specification for both VPP and VCMR. As an example, let's use an input driver with an amplitude (VSWING) of 200mV and a VOH level at 2V. Will this work? First, the VSWING should be verified that it is within the VPP specification. Yes, 200mV falls between 0.15V and 1.3V. Second, the VOH of the signal must fall within the VCMR range. Assuming the VCC is 3.3V and VEE is 0V, the VCMR range will be 0.5V and 2.45V. Again, 2V fall within the VCMR range. Both of the conditions are met. This is a valid input. Though not specified, it is not recommended that the VIL goes below VEE. This could happen with the VPP at 1.3V and the VIH at VEE+0.5. That would put the VIL at 800mV below VEE.

Limitations of VCMR and VPP

This section will describe the limitation of both VCMR and v from a circuit perspective. When VCMR is referenced to VIH, the analysis is purely DC. Some inputs also reference VCMR to the input signals cross-point. This would be a similar except it would be an AC analysis.

Figure 3. Simplified Typical Differential Input Interface Circuit



For the following analysis, refer to Figure 3. In determining VPP, both VPP(min) and VPP(max) specification must be examined. For both cases, VIN+ is greater than VIN-, where VIN+ is a logic high and VIN- is a logic low.

- VPP(min) is determined by the minimum voltage difference required to correctly operate the differential amplifier by keeping the Q1 transistor on and Q2 off.
- VPP(max) is determined by the maximum voltage swing allowable which will not forward bias either Q1 or Q2.

Similar to VPP, both VCMR(max) and VCMR(min) must be examined.

- VCMR(min) is determined by the minimum VCD required to keep the constant current source I1 function properly.
- VCMR(max) is determined by the minimum VAB required to prevent the forward biasing of Q1.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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