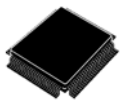
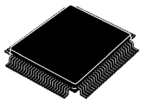
SR5 E1 line of Stellar electrification MCUs — 32-bit Arm® Cortex®-M7 automotive MCU 2x cores, 2 MB Flash, rich analog, high-resolution timer, HSM, ASIL-D



eTQFP100 (14 x 14 x 1.0 mm)



eLQFP176 (24 x 24 x 1.4 mm)

Part number	Package
SR5E1E3	eTQFP100
SR5E1E7	eLQFP176

Features

- AEC-Q100 automotive qualification on going
- SR5 high-performance analog MCUs offering:
  - Digital and analog high-frequency control requested by new wide-bandgap technologies (Silicon Carbide and Gallium Nitride)
  - Superior real-time and functional safety performance (ASIL-D capability)
  - Built-in fast and cost optimized OTA (over-the-air) reprogramming capability (with built-in dual image storage)
  - High-speed security cryptographic services (HSM)

Cores

- 2x 32-bit Arm® Cortex®-M7 with double-precision FPU, L1 cache and DSP instructions
  - Split-lock configuration, allowing either 2 cores in parallel or 1 core in lockstep configuration
- 2 DMA engines in lockstep configuration

Memories

- Up to 2 MB on-chip Flash memory with read while write support
  - 1920 KB code Flash memory split in two banks allowing 960 KB OTA reprogramming support
  - 160 KB HSM dedicated code Flash memory
- 96 KB data Flash memory (64 KB + 32 KB dedicated to HSM)
- 488 KB on-chip general-purpose SRAM:
  - 2x 32 KB instruction TCM + 2x 64 KB data TCM
  - 256 KB system RAM
  - 40 KB HSM dedicated system RAM

Security: hardware security module (HSM)

- On-chip high-performance security module with dedicated RAM and Flash
- Based on Cortex®-M0+ core
- Hardware accelerator for symmetric cryptography

Safety: comprehensive new generation ASIL-D safety concept

- State of the art safety measures at all level of the architecture for most efficient implementation of ISO26262 ASIL-D functionalities
- FCCU for collection and reaction to failure notifications with enhanced configurability
- Memory error management unit (MEMU) for collection and reporting of error events in memories
- Cyclic redundancy check (CRC) unit

Enhanced peripherals for fast control loop capability

- 12 Timers:
  - 2x HRTIM (high-resolution and complex waveform builder)
  - 2x advanced control timers
  - 2x 32-bit + 4x 16-bit general purpose timers
  - 2x basic timers
- Enhanced analog-to-digital converter system with:
  - 5 SAR analog converters
  - 2 sigma-delta analog converters
- Digital-to-analog converters (DAC)
  - 2 buffered external channels
  - 8 unbuffered internal channels
- 8 comparators
- Hardware accelerator
  - 1x CORDIC for trigonometric functions acceleration

Communication interfaces

- 4 modular controller area network (MCAN) modules, all supporting flexible data rate (ISO CAN-FD)
- 3 UART modules with LIN functionality
- 4 serial peripheral interface (SPI) modules, 2 multiplexed with I²S interfaces
- 2 I²C modules

Advanced debug and trace for high-performance automotive application development

- Built around Arm® CoreSight™-600
- Debug interface: Arm® CoreSight™ JTAG (IEEE 1149.1) or SWD
- Embedded trace FIFO for both on- and off-chip tracing
- Trace port for off-chip tracing: parallel trace port configurable from 1 to 8 data lines

1 Introduction

1.1 Document overview

This document provides a summary of the target specification and features of the SR5E1x devices. For detailed information, refer to the device Datasheet and device Reference manual.

Note: For information on the Cortex®-M7 and Cortex®-M0+ cores refer to the Cortex®-M7 and Cortex®-M0+ technical reference manuals, available from the www.arm.com website.

arm

1.2 Description

The SR5E1x MCU family has been designed to meet the enhanced digital control and high-performance analog requested by the new wide band gap power technologies, silicon carbide and GAN, from power conversion applications such as on-board charger and DC/DC converters as well as advanced motor control like traction inverter applications.

SR5E1x also offers superior real-time and safe performance with highest ASIL-D capability, security cryptographic services (HSM) and high efficiency OTA reprogramming capability.

1.3 Product selector

Table 1. SR5E1x product selector

Features		SR5E1x
Cortex®-M7 cores		2 cores, either decoupled or in lockstep
Frequency in MHz		300
Floating point unit		Single and double precision
Cache (instruction / data) per core in Kbyte		8 / 16
Code Flash in Mbyte	Overall included HSM in Mbyte	2
User code Flash in Kbyte		1920
HSM code NVM in Kbyte		160
Code Flash built-in memory replication for OTA reprogramming (not supported by HSM) in Kbyte		Up to 2x 960
Data Flash in Kbyte	Overall included HSM	96
	User data Flash	64
	HSM data Flash	32
RAM in Kbyte	Overall	488
	TCM (instruction / data)	64 / 128
	User system RAM	256
	HSM system RAM	40
Hardware security module (HSM)		Yes
DMA engines (number of channels)	Engine	2
	Channel	2 x 8
Low power mode and smart wake-up schemes		Yes
LIN and UART		3
CAN (with CAN-FD)		4
SPI		4
Timers	Advanced control	2
	High-resolution	2
	General purpose	2 + 4
	Basic	2
SAR analog converters		5
Sigma-delta analog converters		2
Analog comparators		8
External DAC		2
Debug port	Main debug port (JTAG+SWD)	Yes
	Secondary debug port (SWD)	No
Max temperature (target)	Ambient temperature	125 °C
Junction temperature		150 °C
Packages	QFP100	X
	QFP176	X

Revision history

Table 2. **Document revision history**

Date	Version	Changes
12-Mar-2021	1	Initial release.
31-Jan-2022	2	Initial public release.