ISO7810x High-Performance, 8000-V_{PK} Reinforced Single-Channel Digital Isolator

1 Features

- Signaling Rate: Up to 100 Mbps
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25 V to 5.5 V Level Translation
- Wide Temperature Range: –55°C to 125°C
- Low Power Consumption, Typical 1.8 mA at 1 Mbps
- Low Propagation Delay: 10.7 ns Typical (5 V Supplies)
- Industry leading CMTI (Min): ±100 kV/μs
- Robust Electromagnetic Compatibility (EMC)
- System-Level ESD, EFT, and Surge Immunity
- Low Emissions
- Isolation Barrier Life: > 40 Years
- SOIC-16 Wide Body (DW) and Extra-Wide Body (DWW) Package Options
- Safety-Related Certifications:
  - 8000 V_{PK} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 5.7 kV_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
  - TUV Certification per EN 61010-1 and EN 60950-1
  - All DW Package Certifications Complete; DWW Package Certifications Complete per UL, VDE, and TUV and Planned for CSA and CQC

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment
- Hybrid Electric Vehicles

3 Description

The ISO7810x device is a high-performance, single-channel digital isolator with 8000 V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, CQC, and TUV. The isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os.

The isolation channel has a logic input and output buffer separated by silicon dioxide (SiO_2) insulation barrier. If the input power or signal is lost, the default output is *high* for the ISO7810 and *low* for the ISO7810F device. See the *Device Functional Modes* section for further details.

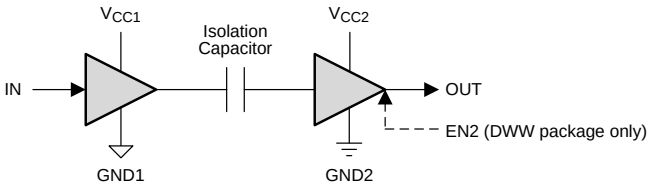
Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO7810x device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO7810x device is available in 16-pin SOIC wide-body (DW) and extra-wide body (DWW) packages.The DWW package option comes with enable pin which can be used to put the output in high impedance state for multi-master driving applications and to reduce power consumption.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7810 ISO7810F	DW (16)	10.30 mm × 7.50 mm
	DWW (16)	10.30 mm × 14.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2015) to Revision B **Page**

- Changed *Features* From: Low Power Consumption, Typical 1.8 mA per Channel at 1 Mbps To: Low Power Consumption, Typical 1.8 mA at 1 Mbps ... 1
- Changed *Features* From: Low Propagation Delay: 11 ns Typical To: Low Propagation Delay: 10.7 ns Typical ... 1
- Changed *Features* From: Safety and Regulatory Approvals To: Safety-Related Certifications ... 1
- Added the extra-wide body package (16 pin SOIC [DWW]) option ... 1
- Changed the INA, OUTA, V_{CCI}, and V_{CCO} pin names to IN, OUT, V_{CC1}, and V_{CC2} (respectively) and updated the pin out drawings, *Pin Functions* table, and other figures to match ... 4
- Moved Junction temperature From *Recommended Operating Conditions* To *Absolute Maximum Ratings* ... 5
- Changed the *Thermal Information* values for the DW package and add the values for the DWW package ... 6
- Changed the values in the *Power Rating* table ... 6
- Moved *Insulation Characteristics* to the *Specifications* section ... 7
- Changed C_{IO} Specification From: 2 pF To: ~0.75 pF ... 7
- Moved *Regulatory Information* to the *Specifications* section ... 8
- Moved *Safety Limiting Values* to the *Specifications* section ... 8
- Changed the minimum CMTI value from 50 to 100 and deleted the maximum value in the 5-V and 3.3-V electrical characteristics tables. Also added V_{CM} to the test conditions ... 9
- Changed the maximum value for the supply current, AC parameter at 100 Mbps in all of the electrical characteristics tables ... 9
- Changed the minimum CMTI value from 70 to 100 and deleted the maximum value in the 2.5-V electrical characteristics table. Also added V_{CM} to the test conditions ... 11
- Added the disable and enable propagation delay parameters to all of the switching characteristics tables ... 12

Revision History (continued)

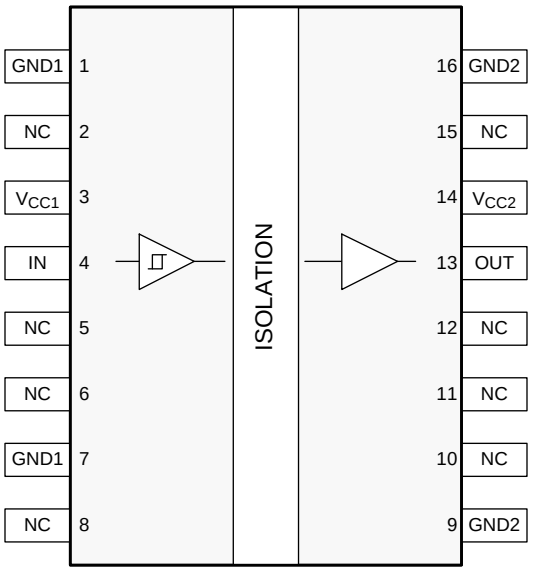
- Changed t_{fs} To: t_{DO} in *Switching Characteristics—5-V Supply* 12
- Changed t_{fs} To: t_{DO} in *Switching Characteristics—3.3-V Supply* 12
- Changed t_{fs} To: t_{DO} in *Switching Characteristics—2.5-V Supply* 13
- Added the *Insulation Characteristics Curves* section 14
- Added the lifetime projection curves for the DW and DWW packages in the *Insulation Characteristics Curves* section 14
- Added Figure 15 in the *Parameter Measurement Information* section 17
- Changed text "dual-channel digital isolator" To: "single-channel digital isolator" in *Application Information* 21
- Changed text "DC-DC converters" To: "transformer driver" in the *Typical Application* section 21
- Changed Figure 20 21

Changes from Original (July 2015) to Revision A **Page**

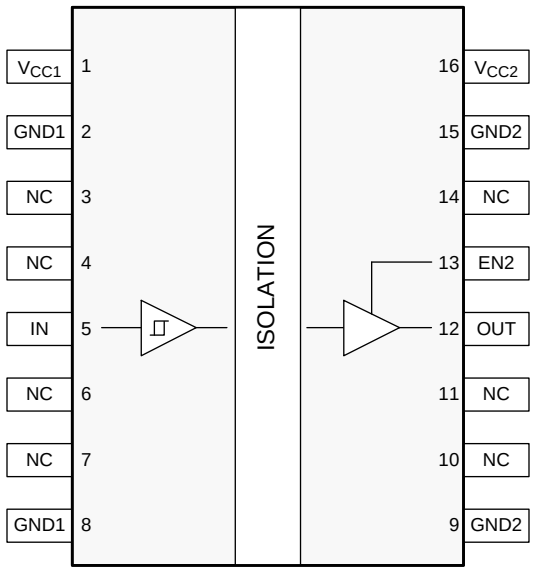
- Changed From: 1-page Product Preview To: Production datasheet 1

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



DWW Package
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DW	DWW		
EN2	—	13	I	Output enable 2. Output pin on side 2 is enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	1, 7	2, 8	—	Ground connection for V_{CC1}
GND2	9, 16	9, 15	—	Ground connection for V_{CC2}
IN	4	5	I	Input channel
NC	2, 5, 6, 8, 10, 11, 12, 15	3, 4, 6, 7, 10, 11, 14	—	Not connected
OUT	13	12	O	Output channel
V_{CC1}	3	1	—	Power supply, side 1
V_{CC2}	14	16	—	Power supply, side 2

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Supply voltage(2)	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage	IN, OUT, EN2	–0.5	V_{CC} + 0.5(3)	V
Output current, I_O		–15	15	mA
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CC2} = 5 V	–4			mA
		V_{CC2} = 3.3 V	–2			
		V_{CC2} = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CC2} = 5 V			4	mA
		V_{CC2} = 3.3 V			2	
		V_{CC2} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CC1}		V_{CC1}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CC1}	V
t_{ui}	Input pulse duration		7			ns
DR	Signaling rate		0		100	Mbps
T_A	Ambient temperature		–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ISO7810x		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89	92.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.5	53.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.6	62.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	23.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.1	62.2	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, input a 50 MHz 50% duty cycle square wave			50	mW
P_{D1}	Maximum power dissipation by side-1				12.5	mW
P_{D2}	Maximum power dissipation by side-2				37.5	mW

6.6 Insulation Characteristics

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	>14.5	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	>8	>14.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group		I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	I–IV	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 (2)					
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification) t= 1 s (100% production)	8000	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	8000	V_{PK}
V_{IORM}	Maximum repetitive peak isolation voltage		2121	2828	V_{PK}
V_{IOWM}	Maximum isolation working voltage	Time dependent dielectric breakdown (TDDB) test; see Figure 1 and Figure 2	1500	2000	V_{RMS}
			2121	2828	V_{DC}
V_{PR}	Input-to-output test voltage	Method a, After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	2545	3394	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial Discharge < 5 pC	3394	4525	
		Method b1,After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% Production test) Partial discharge < 5 pC	3977	5303	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.75	~0.75	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max	$>10^{11}$	$>10^{11}$	Ω
R_S	Isolation resistance	V_{IO} = 500 V at T_S	$>10^9$	$>10^9$	Ω
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 s (100% production)	5700	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Regulatory Information

DW package certifications are complete. DWW package certifications completed for UL, VDE, and TUV and planned for CSA and CQC.

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011 /A2:2013
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK}(DW package), 2828 V_{PK} (DWW package); Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage	Single protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW package) and 1000 V_{RMS} (DWW package) 5700 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011 /A2:2013 up to working voltage of 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 89°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 3			255	mA
		$R_{\theta JA}$ = 89°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 3			390	
		$R_{\theta JA}$ = 89°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 3			511	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 89°C/W, T_J = 150°C, T_A = 25°C, see Figure 5			1404	mW
T_S	Maximum safety temperature				150	°C
DWW PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 92.2°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 4			246	mA
		$R_{\theta JA}$ = 92.2°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 4			377	
		$R_{\theta JA}$ = 92.2°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 4			493	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 92.2°C/W, T_J = 150°C, T_A = 25°C, see Figure 6			1356	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a high-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 13	V_{CC2} – 0.4	V_{CC2} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 13		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CC1}			V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at IN or EN2			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at IN or EN2	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1500 V; see Figure 16	100			kV/µs
C_I	Input capacitance (1)	V_I = V_{CC}/2 + 0.4 × sin (2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable (DWW package only)	EN2 = 0 V, V_I = 0 V (Devices with suffix F), V_I = V_{CC1} (Devices without suffix F)		I_{CC1}		0.6	1.1	mA
			I_{CC2}		0.16	0.3	
	EN2 = 0 V, V_I = V_{CC1} (Devices with suffix F), V_I = 0 V (Devices without suffix F)		I_{CC1}		1.8	2.7	
			I_{CC2}		0.16	0.3	
Supply current - DC signal	V_I = 0 V (Devices with suffix F), V_I = V_{CC1} (Devices without suffix F)		I_{CC1}		0.6	1.1	mA
			I_{CC2}		0.6	1.1	
	V_I = V_{CC1} (Devices with suffix F), V_I = 0 V (Devices without suffix F)		I_{CC1}		1.8	2.7	
			I_{CC2}		0.7	1.1	
Supply current - AC signal	Input signal switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.2	1.9	mA
			I_{CC2}		0.6	1.1	
		10 Mbps	I_{CC1}		1.2	1.9	
			I_{CC2}		1.1	1.6	
		100 Mbps	I_{CC1}		1.3	2	
			I_{CC2}		5.7	7.3	

6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 13	V_{CC2} – 0.4	V_{CC2} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 13		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CC1}			V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at IN or EN2			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at IN or EN2	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1500 V; see Figure 16	100			kV/µs

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable (DWW package only)	EN2 = 0 V, V_I = 0 V (Devices with suffix F), V_I = V_{CC1} (Devices without suffix F)		I_{CC1}		0.6	1.1	mA
			I_{CC2}		0.16	0.3	
	EN2 = 0 V, V_I = V_{CC1} (Devices with suffix F), V_I = 0 V (Devices without suffix F)		I_{CC1}		1.8	2.7	
			I_{CC2}		0.16	0.3	
Supply current - DC signal	V_I = 0 V (Devices with suffix F), V_I = V_{CC1} (Devices without suffix F)		I_{CC1}		0.6	1.1	mA
			I_{CC2}		0.6	1	
	V_I = V_{CC1} (Devices with suffix F), V_I = 0 V(Devices without suffix F)		I_{CC1}		1.8	2.7	
			I_{CC2}		0.6	1.1	
Supply current - AC signal	Input signal switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.2	1.9	mA
			I_{CC2}		0.6	1.1	
		10 Mbps	I_{CC1}		1.2	1.9	
			I_{CC2}		0.9	1.4	
		100 Mbps	I_{CC1}		1.3	2	
			I_{CC2}		4.1	5.4	

6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 13	V_{CC2} – 0.4	V_{CC2} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 13		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CC1}			V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at IN or EN2			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at IN or EN2	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1500 V; see Figure 16	100			kV/µs

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current, - disable (DWW package only)	EN2 = 0 V, V_I = 0 V (Devices with suffix F), V_I = V_{CC1} (Devices without suffix F)		I_{CC1}		0.6	1.1	mA
			I_{CC2}		0.16	0.3	
	EN2 = 0 V, V_I = V_{CC1} (Devices with suffix F), V_I = 0 V (Devices without suffix F)		I_{CC1}		1.8	2.7	
			I_{CC2}		0.16	0.3	
Supply current - DC signal	V_I = 0 V (Devices with suffix F), V_I = V_{CCx} (Devices without suffix F)		I_{CC1}		0.6	1.1	mA
			I_{CC2}		0.6	1	
	V_I = V_{CCx} (Devices with suffix F), V_I = 0 V(Devices without suffix F)		I_{CC1}		1.8	2.7	
			I_{CC2}		0.6	1.1	
Supply current - AC signal	Input signal switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.2	1.9	mA
			I_{CC2}		0.6	1.1	
		10 Mbps	I_{CC1}		1.2	1.9	
			I_{CC2}		0.9	1.3	
		100 Mbps	I_{CC1}		1.3	2	
			I_{CC2}		3.3	4.4	

6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 13	6	10.7	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				0.6	4.6	ns
$t_{sk(pp)}$	Part-to-part skew time(2)					4.5	ns
t_r	Output signal rise time		See Figure 13		2.4	3.9	ns
t_f	Output signal fall time				2.4	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7810DWW and ISO7810FDWW		See Figure 14		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7810DWW and ISO7810FDWW				12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO7810DWW			10	20	ns
		ISO7810FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO7810DWW			2	2.5	µs
		ISO7810FDWW			10	20	ns
t_{DO}	Default output delay time from input power loss		Measured from the time V_{CC} goes below 1.7 V. See Figure 15		0.2	9	µs
t_{ie}	Time interval error		2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 13	6	10.8	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				0.7	4.7	ns
$t_{sk(pp)}$	Part-to-part skew time(2)					4.5	ns
t_r	Output signal rise time		See Figure 13		1.3	3	ns
t_f	Output signal fall time				1.3	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7810DWW and ISO7810FDWW		See Figure 14		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7810DWW and ISO7810FDWW				17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO7810DWW			17	32	ns
		ISO7810FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO7810DWW			2	2.5	µs
		ISO7810FDWW			17	32	ns
t_{DO}	Default output delay time from input power loss		Measured from the time V_{CC} goes below 1.7 V. See Figure 15		0.2	9	µs
t_{ie}	Time interval error		2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

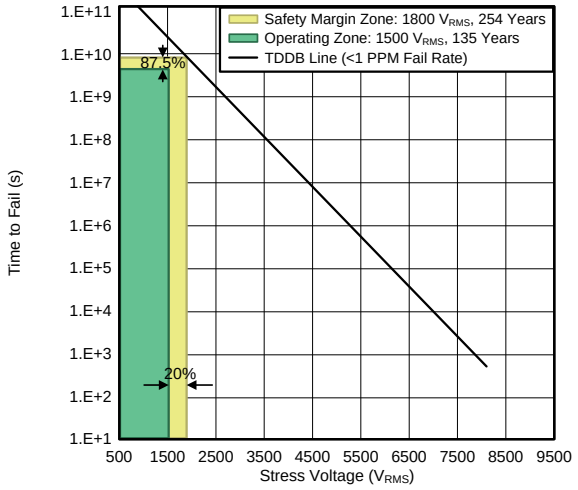
6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 13	7.5	11.7	17.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 13		0.7	4.7	ns
$t_{sk(pp)}$	Part-to-part skew time(2)					4.5	ns
t_r	Output signal rise time		See Figure 13		1.8	3.5	ns
t_f	Output signal fall time		See Figure 13		1.8	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7810DWW and ISO7810FDWW		See Figure 14		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7810DWW and ISO7810FDWW		See Figure 14		22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO7810DWW	See Figure 14		18	45	ns
		ISO7810FDWW	See Figure 14		2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO7810DWW	See Figure 14		2	2.5	µs
		ISO7810FDWW	See Figure 14		18	45	ns
t_{DO}	Default output delay time from input power loss		Measured from the time V_{CC} goes below 1.7 V. See Figure 15		0.2	9	µs
t_{ie}	Time interval error		2^{16} – 1 PRBS data at 100 Mbps		1		ns

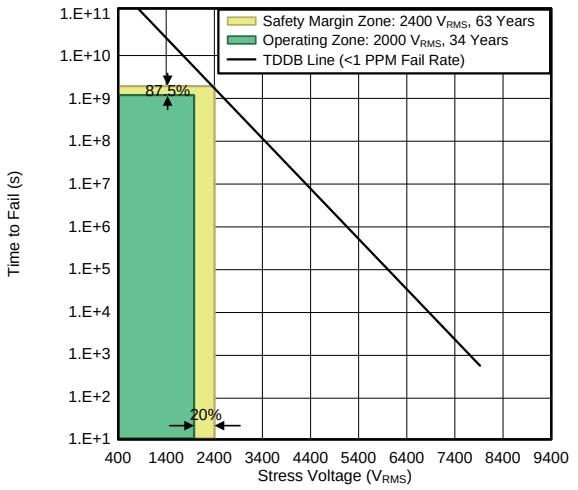
(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves



T_A upto 150°C
Operating lifetime = 135 years
Stress-voltage frequency = 60 Hz
Isolation working voltage = 1500 V_{RMS}

Figure 1. Reinforced Isolation Capacitor Lifetime Projection for Devices in DW Package



T_A upto 150°C
Operating lifetime = 34 years
Stress-voltage frequency = 60 Hz
Isolation working voltage = 2000 V_{RMS}

Figure 2. Reinforced Isolation Capacitor Lifetime Projection for Devices in DWW Package

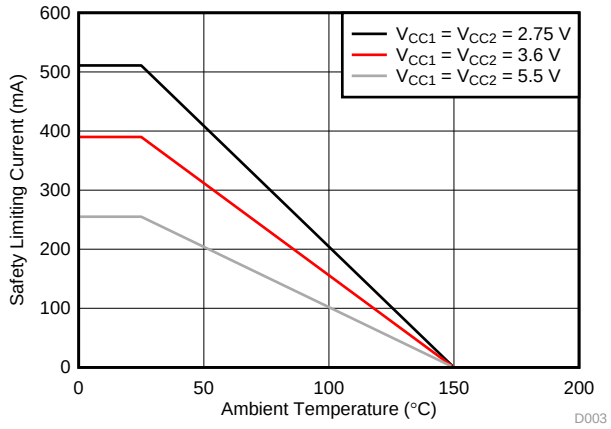


Figure 3. Thermal Derating Curves for Safety Limiting Current for DW Package

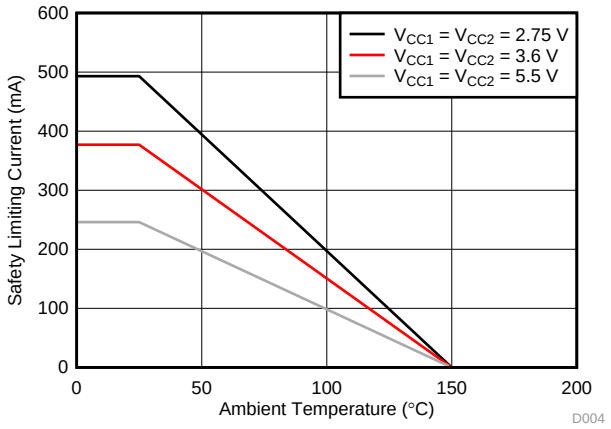


Figure 4. Thermal Derating Curves for Safety Limiting Current for DWW Package

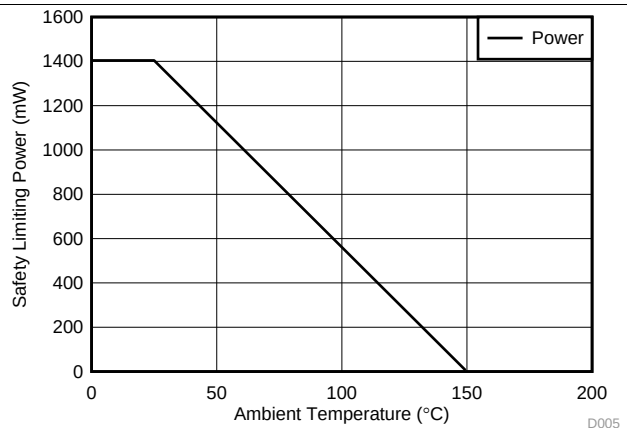


Figure 5. Thermal Derating Curve for Safety Limiting Power for DW Package

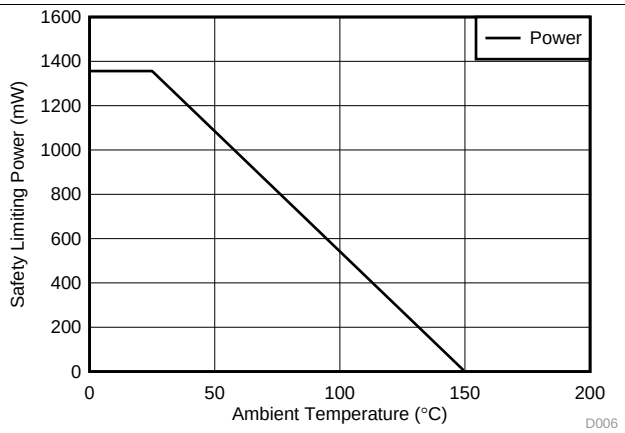


Figure 6. Thermal Derating Curve for Safety Limiting Power for DWW Package

6.19 Typical Characteristics

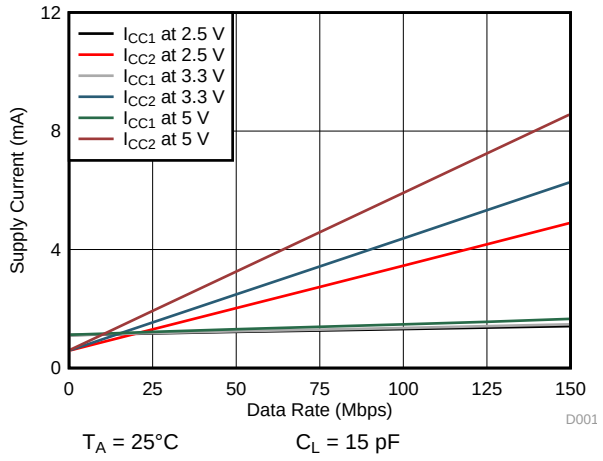


Figure 7. Supply Current vs Data Rate (With 15-pF Load)

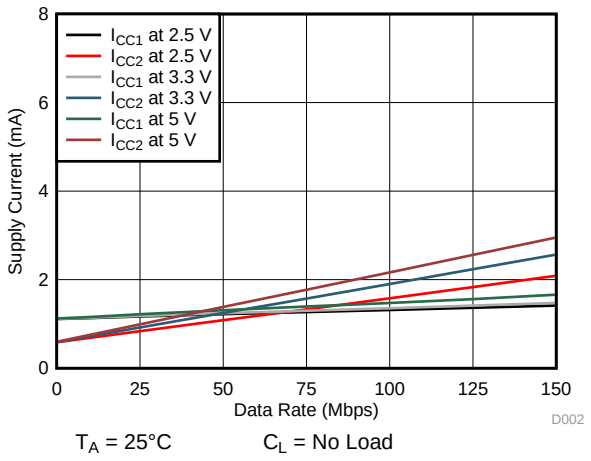


Figure 8. Supply Current vs Data Rate (With No Load)

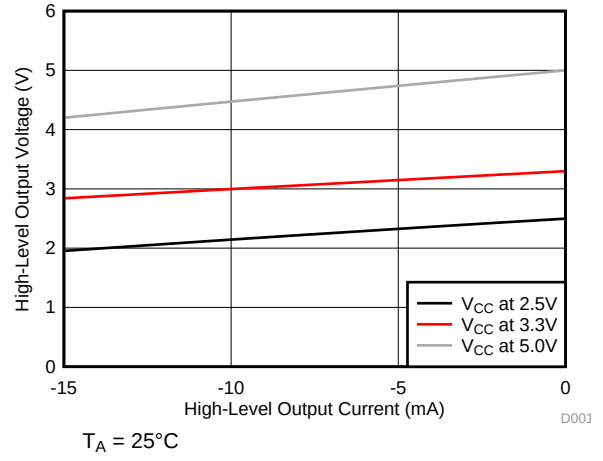


Figure 9. High-Level Output Voltage vs High-level Output Current

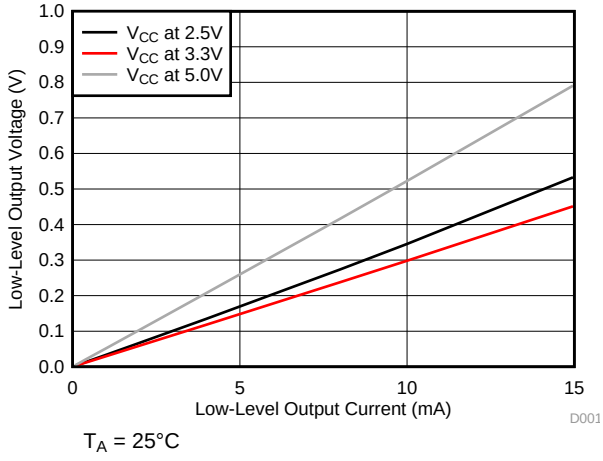


Figure 10. Low-Level Output Voltage vs Low-Level Output Current

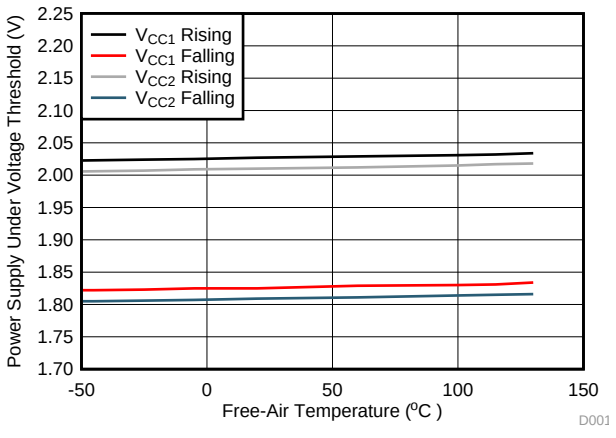


Figure 11. Power Supply Undervoltage Threshold vs Free-Air Temperature

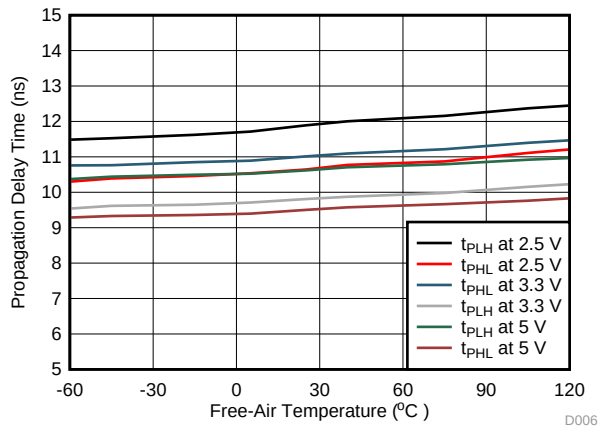
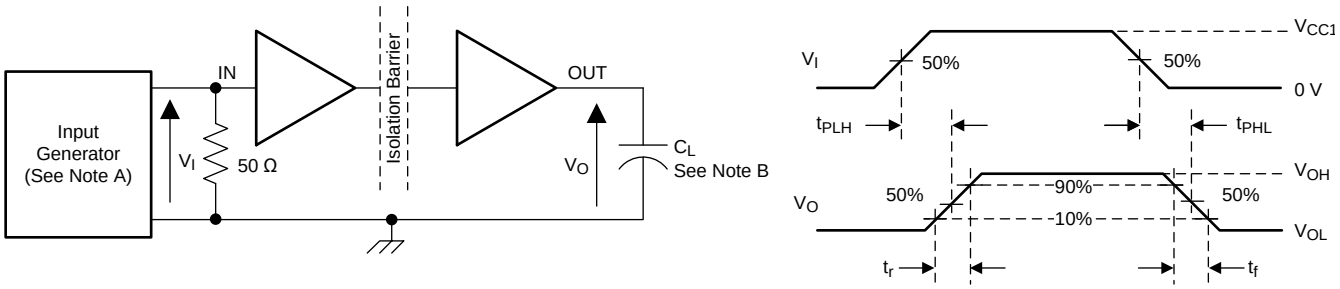


Figure 12. Propagation Delay Time vs Free-Air Temperature

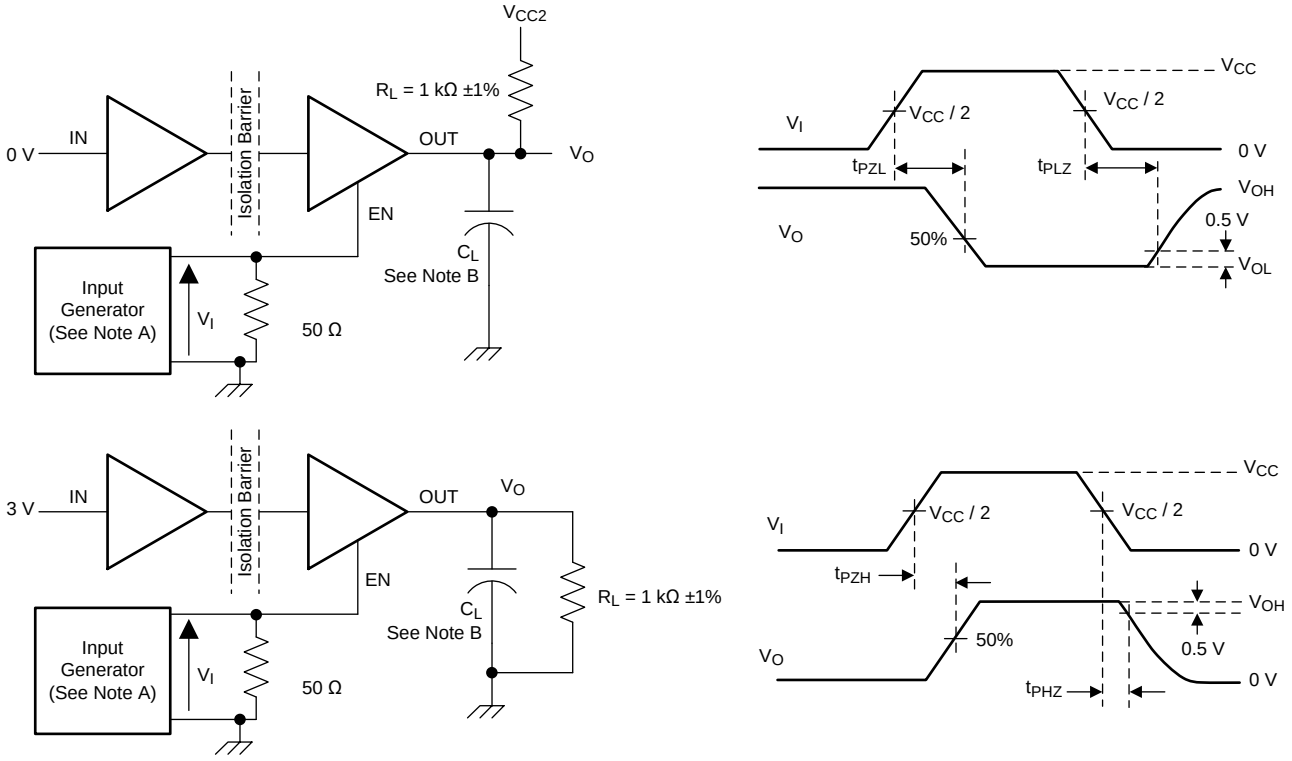
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Switching Characteristics Test Circuit and Voltage Waveforms

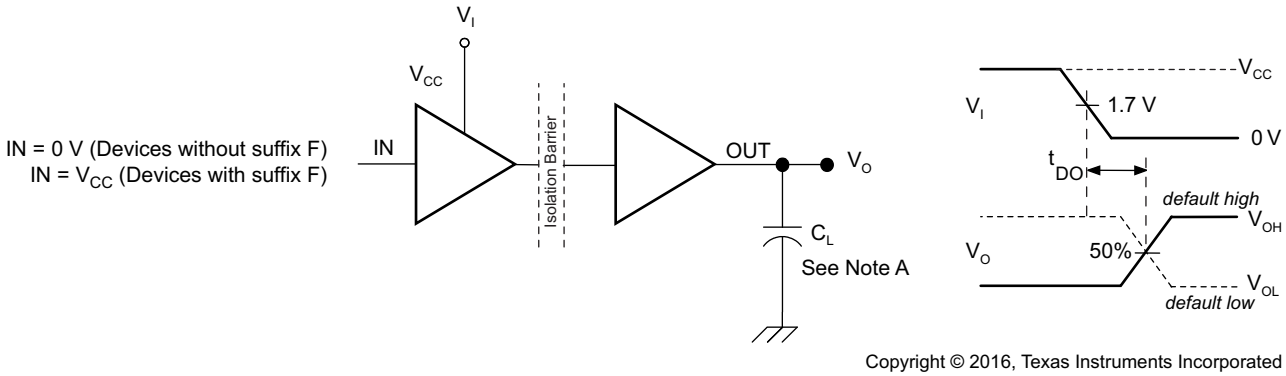


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

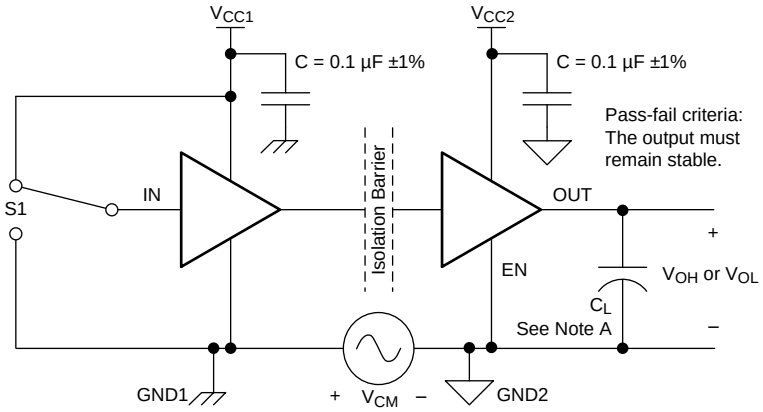
Figure 14. Enable and Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 15. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 16. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7810x device has an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 17, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

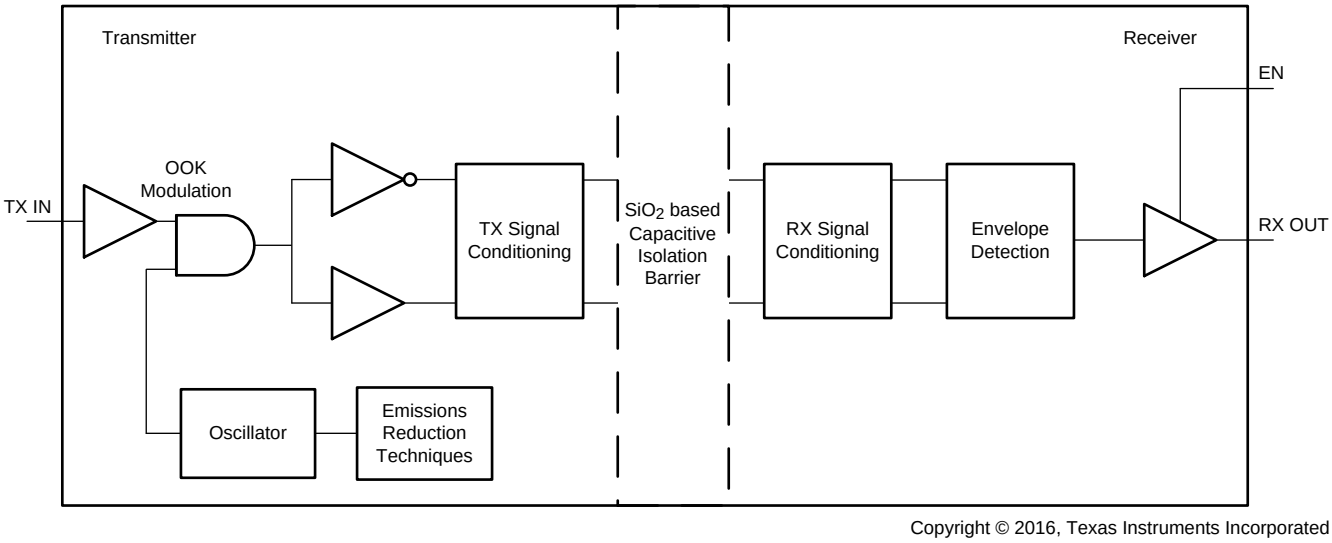


Figure 17. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 18 shows how the ON/OFF keying scheme works.

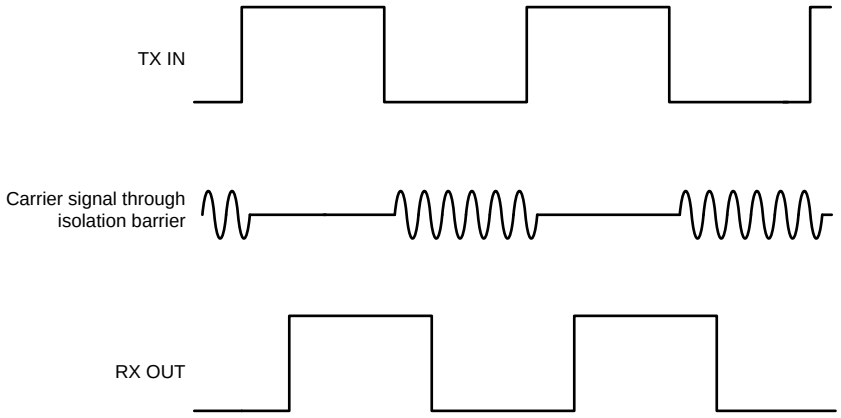


Figure 18. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISO7810 is available in both default output state options to enable a variety of application uses. Table 1 provides an overview of the device features.

Table 1. Device Features

PART NUMBER	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO7810	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	High
ISO7810F	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	Low

(1) See the *Regulatory Information* section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7810x device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the ISO7810x functional modes.

Table 2. Function Table(1)

V_{CC1}	V_{CC2}	INPUT (IN)(2)	OUTPUT (OUT)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When IN is open, the corresponding channel output goes to the default logic state. Default = High for ISO7810 and Low for ISO7810F.
PD	PU	X	Default	Default mode: When V_{CC1} is unpowered, a channel output assumes the logic state based on the selected default option. Default = High for ISO7810 and Low for ISO7810F. When V_{CC1} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CC1} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CC2} is unpowered, a channel output is undetermined (3). When V_{CC2} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CC1}, V_{CC2} < 2.25 V.

8.4.1 Device I/O Schematics

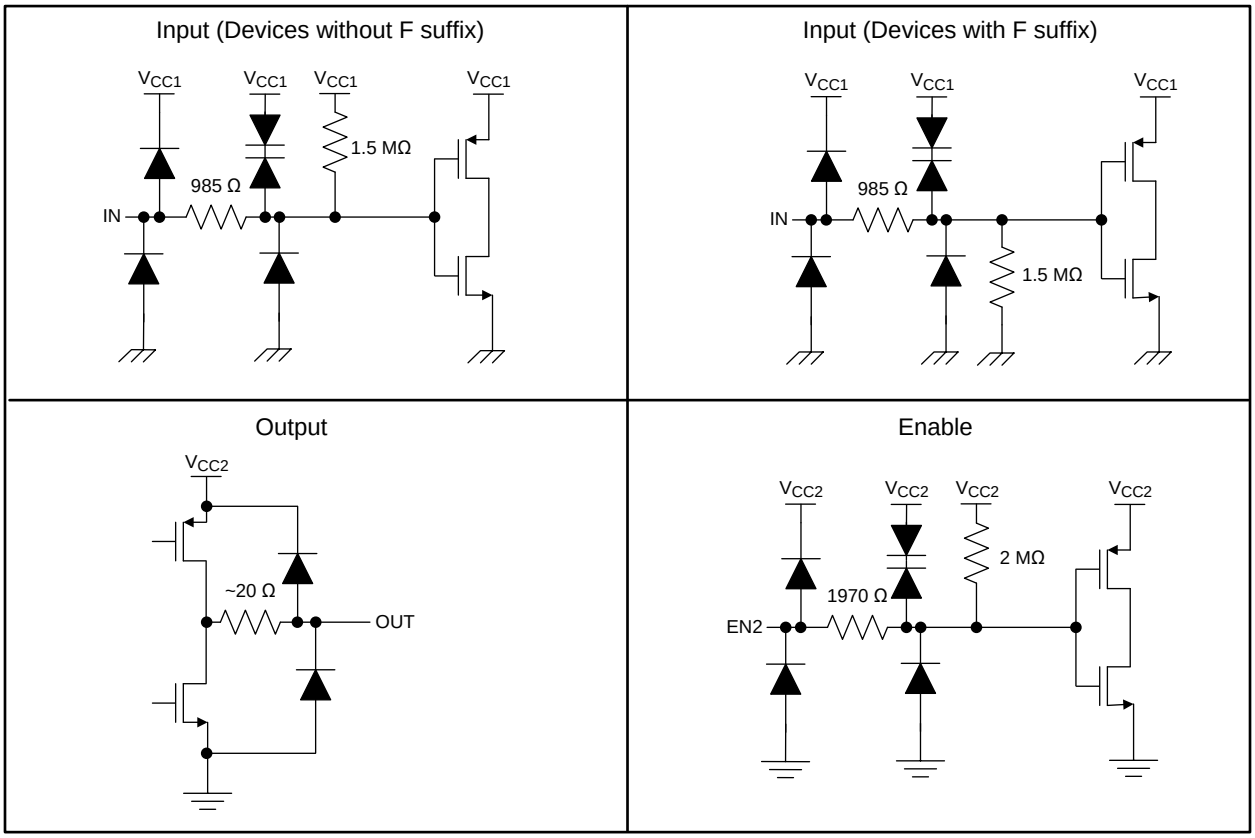


Figure 19. Device I/O Schematics

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7810x device is a high-performance, single-channel digital isolator with a 5.7-kV_{RMS} isolation voltage. The device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7810F device can be used with Texas Instruments' gate driver and transformer driver to create an isolated MOSFET/IGBT drive circuit.

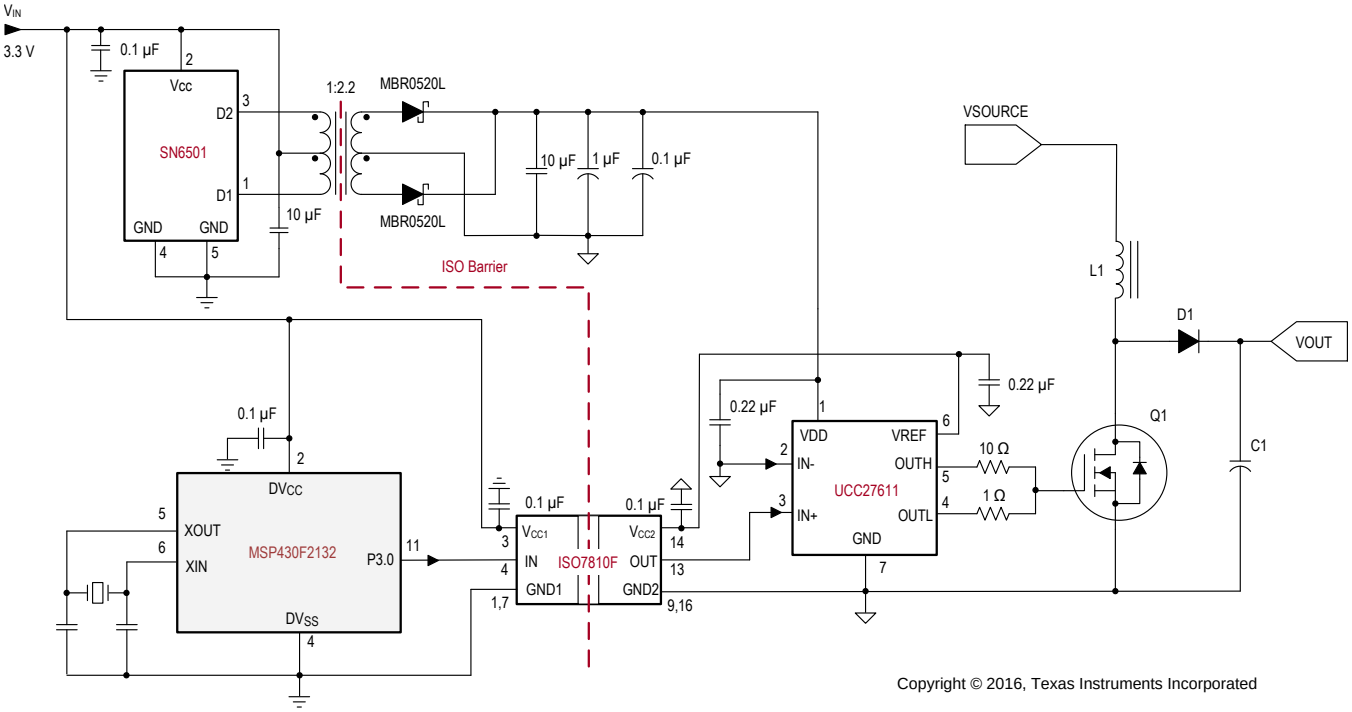


Figure 20. Low-Side Isolated Gate Driver Circuit

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7810x device only requires two external bypass capacitors to operate.

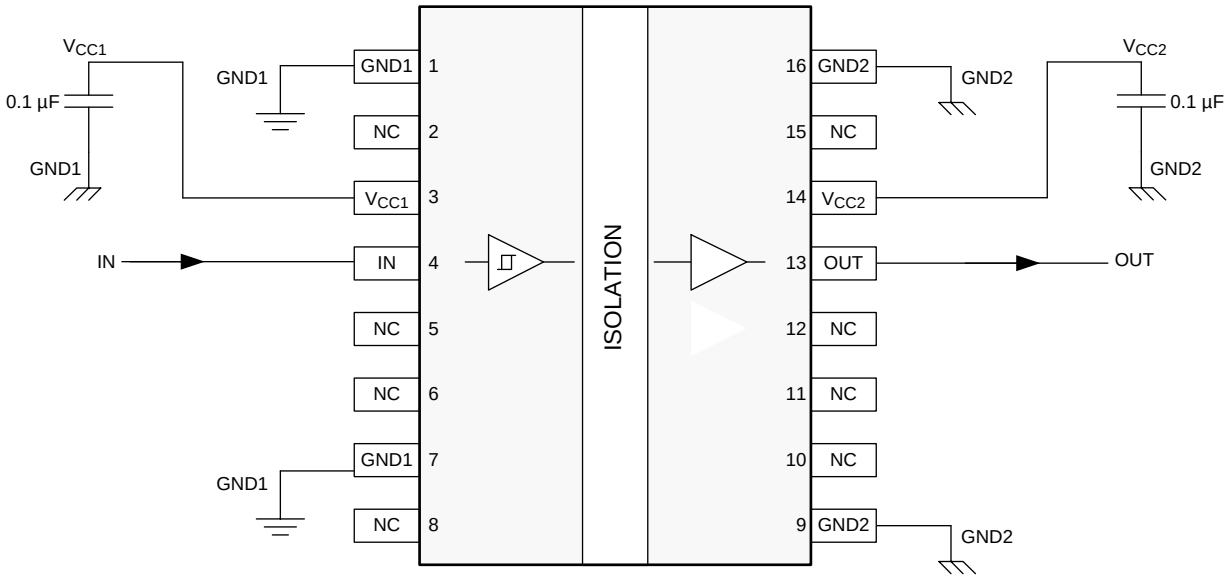


Figure 21. Typical ISO7810DW Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagram of the ISO7810x device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

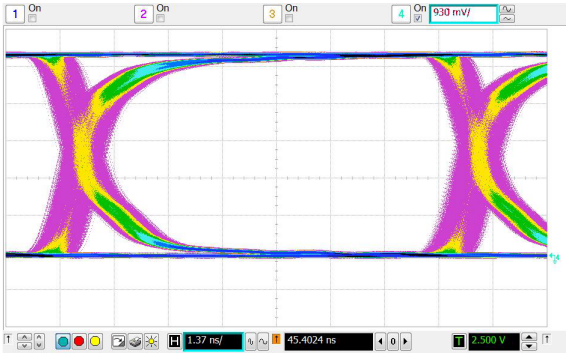


Figure 22. Eye Diagram at 100 Mbps PRBS, 5 V, and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0) .

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 23). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the application note, *Digital Isolator Design Guide* (SLLA284).

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

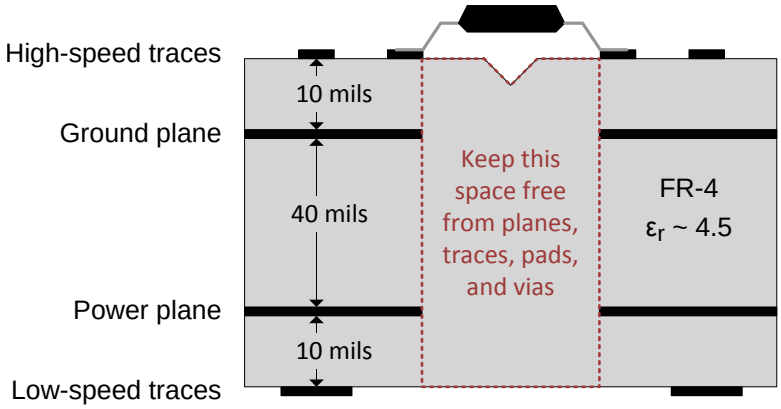


Figure 23. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Isolation Glossary* , SLLA353
- *ISO784xx Quad-Channel Digital Isolator EVM User Guide*, SLAU602
- *Shelf-Life Evaluation of Lead-Free Component Finishes*, SZZA046
- *SN6501 Transformer Driver for Isolated Power Supplies*, SLLSEA0
- *UCC2753x 2.5-A and 5-A, 35-V_{MAX} VDD FET and IGBT Single-Gate Driver*, SLUSBA7
- MSP430F2132 *Mixed Signal Microcontroller*, SLAS578

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7810	Click here	Click here	Click here	Click here	Click here
ISO7810F	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7810DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7810	Samples
ISO7810DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7810	Samples
ISO7810DWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7810	Samples
ISO7810DWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7810	Samples
ISO7810FDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7810F	Samples
ISO7810FDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7810F	Samples
ISO7810FDWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7810F	Samples
ISO7810FDWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7810F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

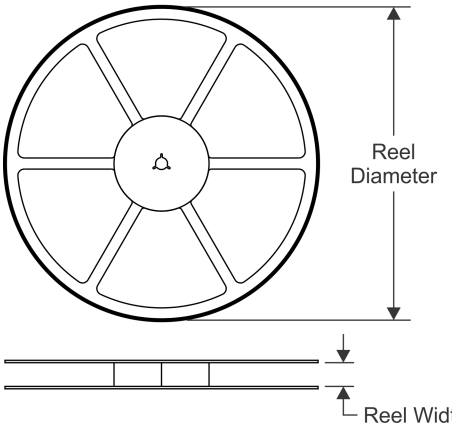
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

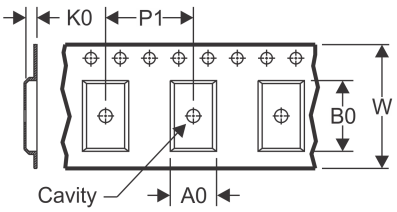
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

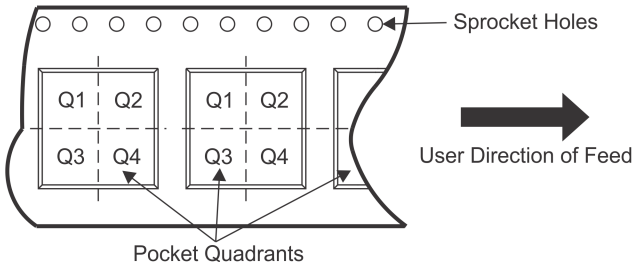


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

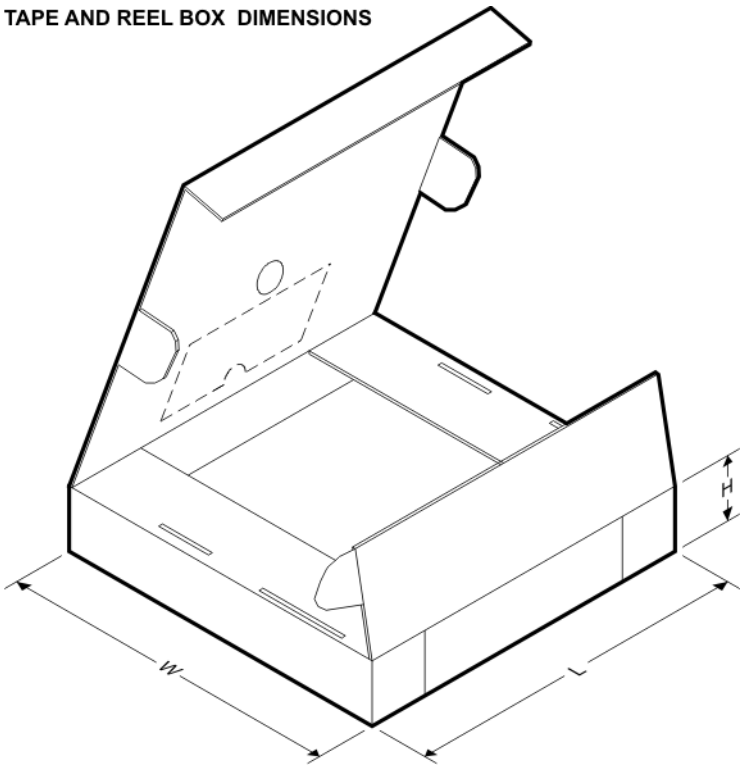
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7810DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7810DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7810FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7810FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

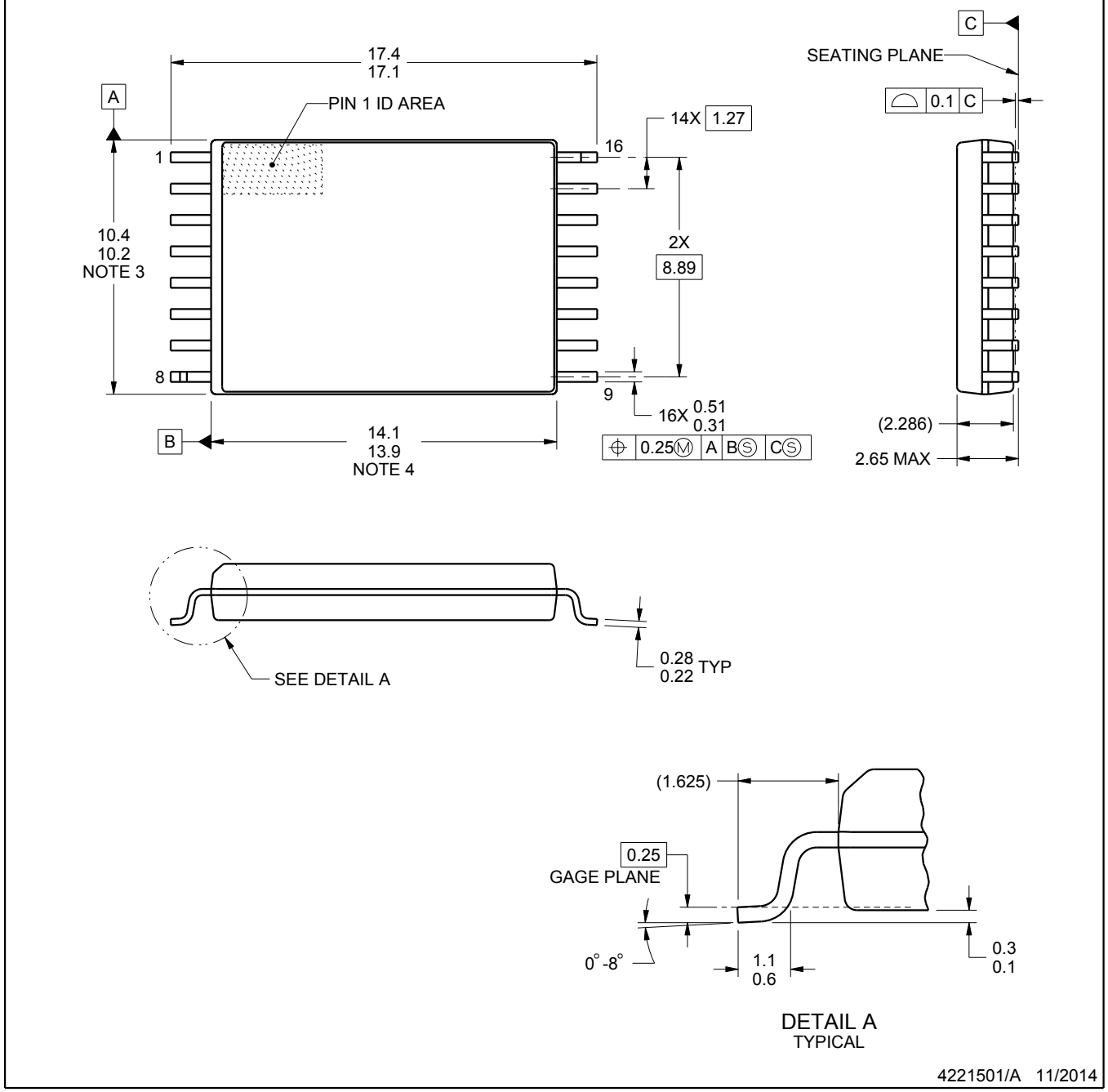
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7810DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7810DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7810FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7810FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

PACKAGE OUTLINE

DWW0016A

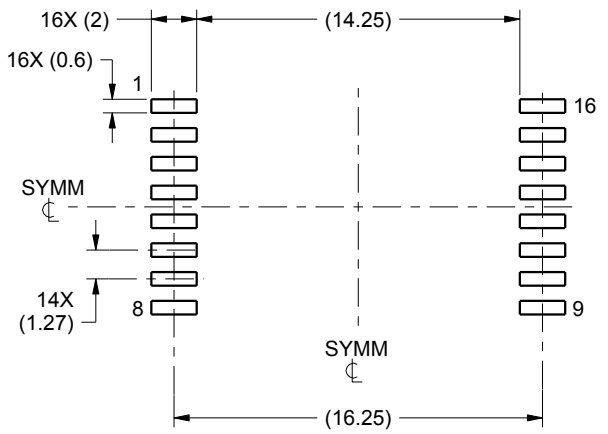
SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE

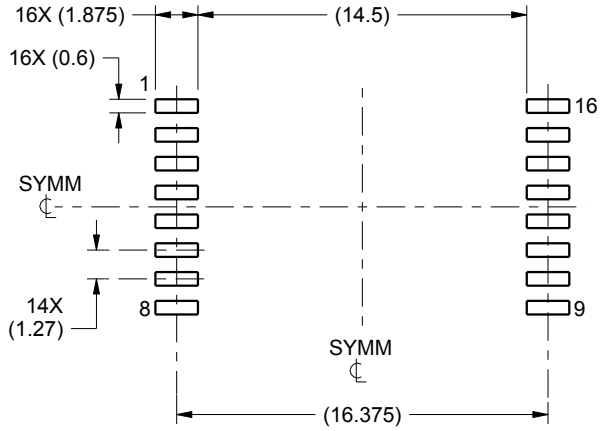


NOTES:

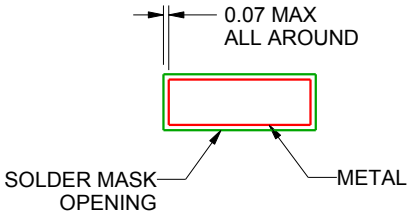
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.



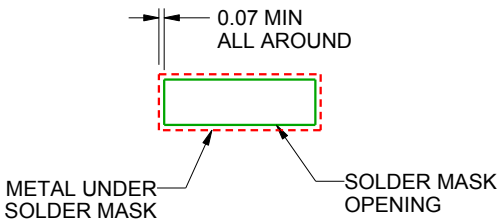
LAND PATTERN EXAMPLE
STANDARD
SCALE:3X



LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X



NON SOLDER MASK
DEFINED
(PREFERRED)



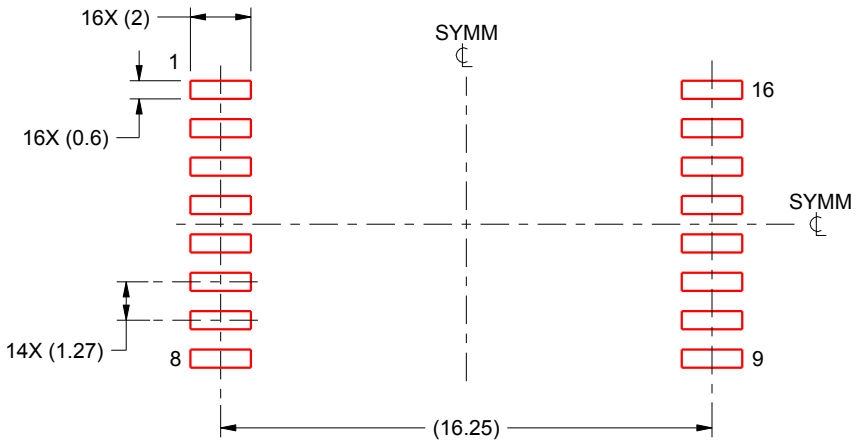
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

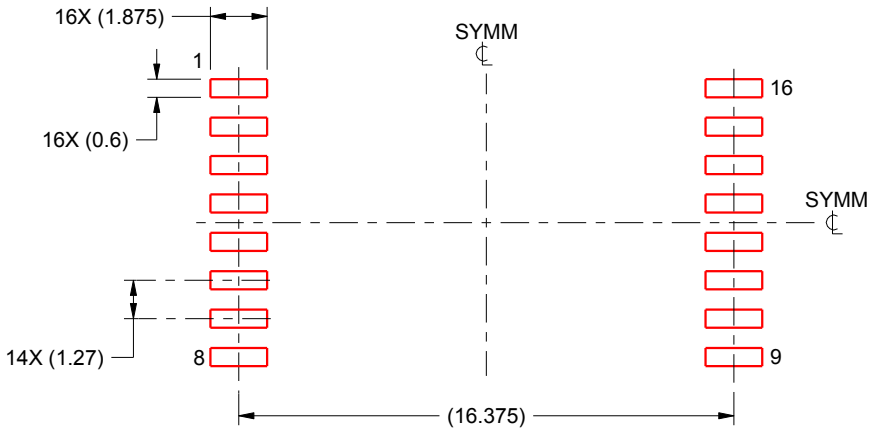
4221501/A 11/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221501/A 11/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

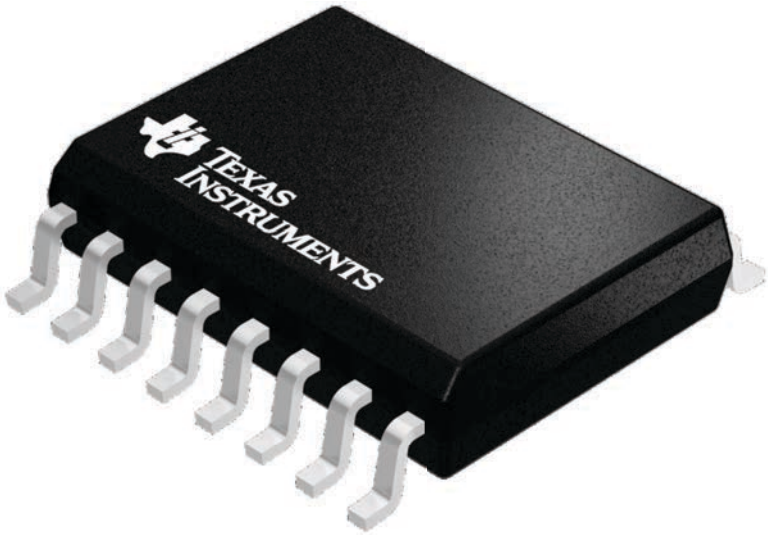
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

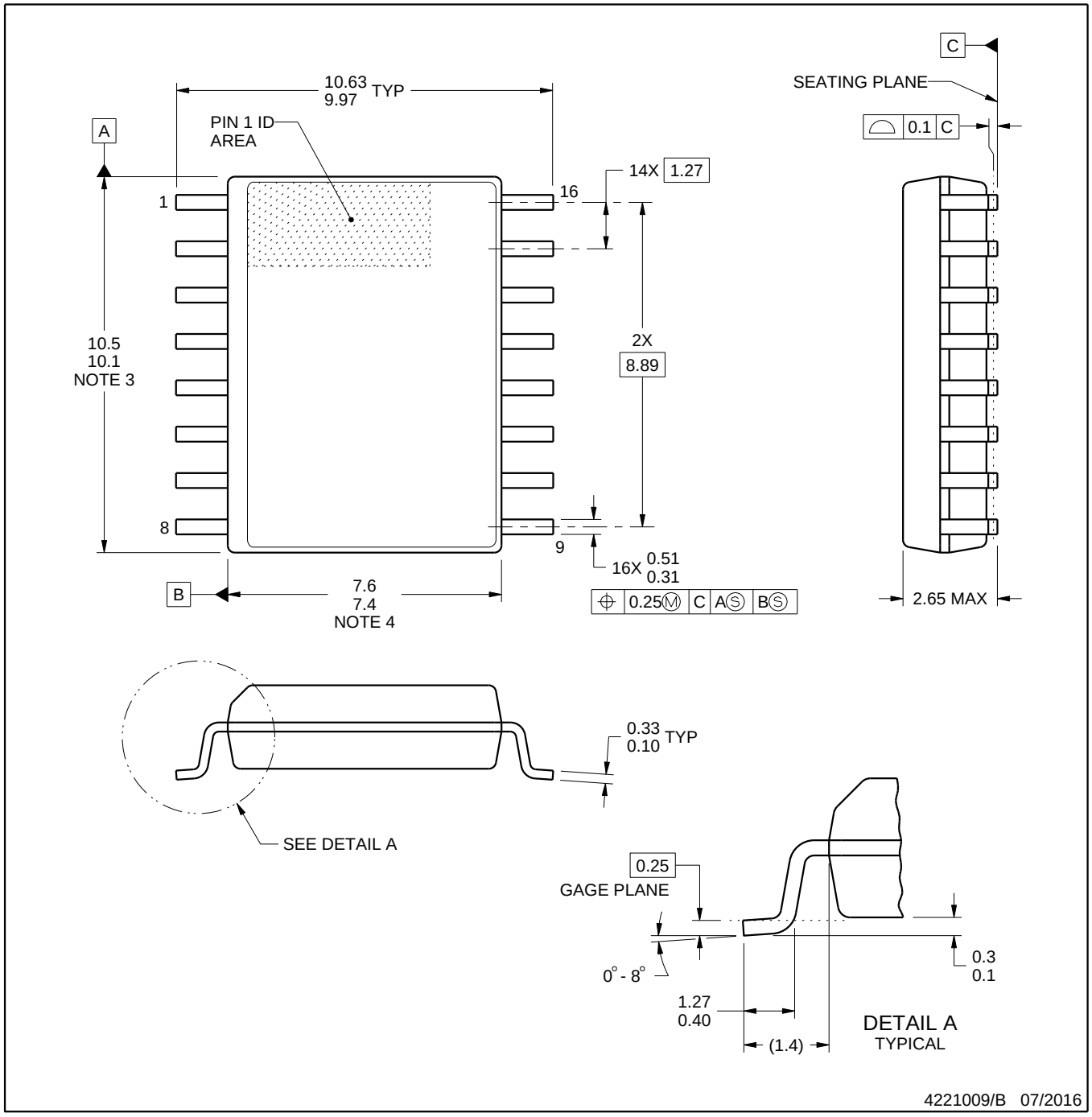
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



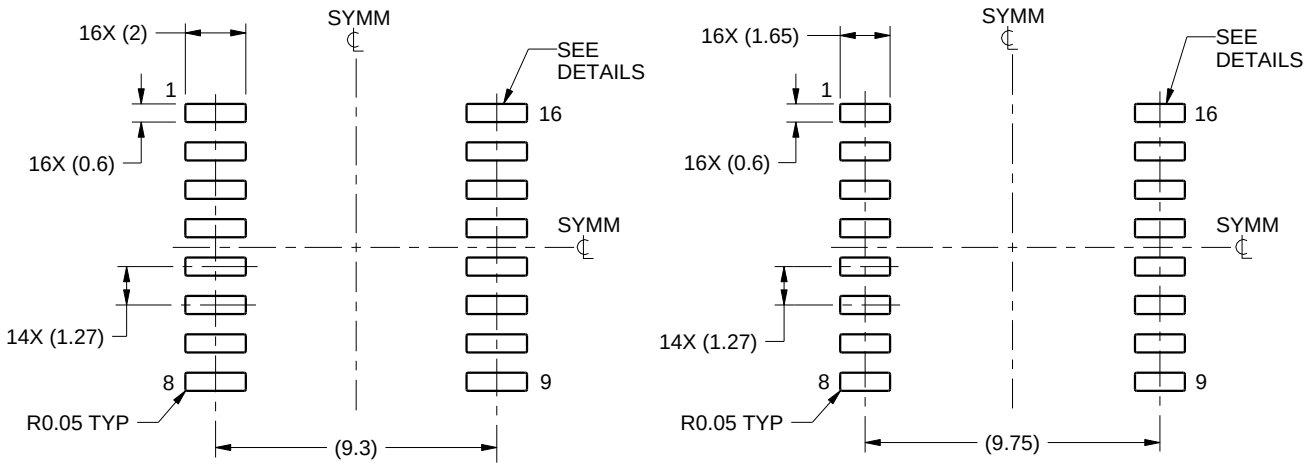
4224780/A

SOIC



NOTES:

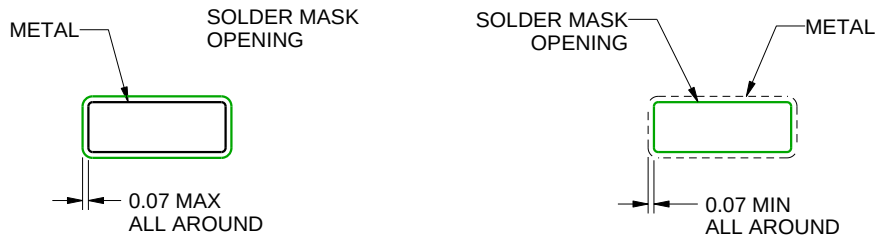
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

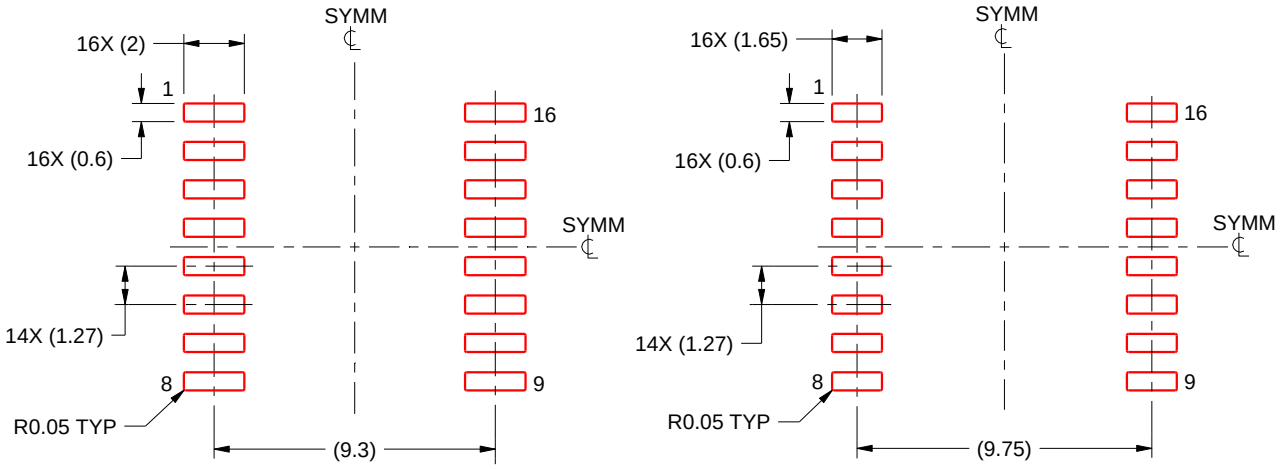
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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