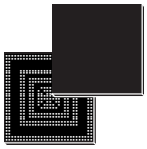
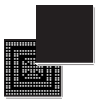
Stellar SR6 P6 line — 32-bit Arm® Cortex®-R52+ automotive integration MCU 6x Cortex®-R52+ cores, 16 MB NVM (2x 15.5 MB “OTA X2”) 2.3 MB RAM, with embedded virtualization, safety and security



FPBGA 516
(25 x 25 mm)



FPBGA 292
(17 x 17 mm)

Part number	Package
SR6P6C8	FPBGA 516
SR6P6C4	FPBGA 292

Features

- AEC-Q100 automotive qualification on going
- SR6 integration MCUs:
  - Have superior real-time and safe performance (with highest ASIL-D capability)
  - Bring HW based virtualization technology to MCUs for simplified multiple SW integrations at optimized performance
  - Have built-in fast and cost effective OTA reprogramming capability (with built-in dual image storage)
  - Offer high speed security cryptographic services, for example for network authentication

Cores

- 32-bit Arm® v8-R compliant CPU cores:
  - 6 Cortex®-R52+ cores (4 of them with checker cores, 2 in split-lock configuration) allowing usage as either 6 cores (4 of them in lockstep configuration) or 5 cores (all of them in lockstep configuration), single precision FPU, new privilege level for real-time virtualization
- 2 Cortex®-M4 multipurpose accelerators (data move and [pre]-processing). One in lockstep configuration
- 4 eDMA engines in lockstep configuration

Memories

- Up to 16 MB on-chip NVM non-volatile memory
  - PCM (phase change memory) as non-volatile memory
  - 15.5 MB code NVM, with embedded memory replication for OTA (over-the-air) reprogramming with up to 2x 15.5 MB
  - 512 KB HSM dedicated code NVM
- 640 KB data NVM (512 KB + 128 KB dedicated to HSM)
- Up to 2304 KB on-chip general-purpose SRAM

Security: hardware security module - 2nd generation

- On-chip high-performance security module with EVITA full support
- Symmetric and asymmetric cryptography processor
- High performance lock-stepped AES-light security sub-system for fast ASIL-D cryptographic services

Safety: comprehensive new generation ASIL-D safety concept

- New state-of-the-art safety measures at all levels of the architecture for most efficient implementation of ISO26262 ASIL-D functionalities
- Complete HW virtualization architecture built on Cortex®-R52+ new privilege mode (best-in class SW isolation, real-time support for multiple virtual machine/applications)

Peripheral, IOs, communication interfaces

- 11 LINFlexD modules
- 2 dual-channel FlexRay controllers
- 10 queued serial peripheral interface (SPIQ) modules
- 4 microsecond channels (MSC) and 2 microsecond plus (MSC-Plus) channels
- 2 SENT modules (15 channels each)
- 2 PSI5 modules (1 channel each)
- Enhanced analog-to-digital converter system with
  - 12 separate 12-bit SAR analog converters (including one supervisor/safety ADC).
  - 4 separate 9-bit SAR analog converters (2 channels each) with fast comparator mode
  - 12 separate 16-bit sigma-delta analog converter with embedded DSP processor on each SD ADC
  - Enhanced interconnection with GTM timer for autonomous ADC/GTM subsystem operation
- Advanced timed I/O capability
  - Generic timer module (GTM4144)
- Communication interfaces
  - 1 ethernet controller 10/100/1000 Mbps, compliant IEEE 802.3-2008: IPv4 and IPv6 checksum modules, AVB, VLAN
  - 11 modular controller area network (MCAN) modules, and 1 time-triggered controller area network (M-TTCAN), all supporting flexible data rate (ISO CAN-FD)
  - 2 CAN-XL interfaces

External memory interfaces

- 2 OctoSPI to support HyperBus™ memory (Flash/RAM) devices

1 Introduction

1.1 Document overview

This document provides a summary of the target specification and features of the SR6P6x devices. For detailed information, refer to the device Datasheet and device Reference manual.

Note: For information on the Cortex®-R52+ and Cortex®-M4 cores refer to the Cortex®-R52+ and Cortex®-M4 technical reference manuals, available from the www.arm.com website.

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1.2 Description

Stellar integration MCUs have been designed to meet the requirements of domain controllers and ECUs with high integration requested in the architectures of connected update-able automated and electrified cars. They have superior real-time and safe performance (with highest ASIL-D capability). Bringing HW based virtualization technology to MCUs, they ease the development and integration of multiple source SW onto the same HW while maximizing the resulting SW performance. They offer high efficiency OTA reprogramming capability with fast new image download and activation at almost no memory overhead thanks to SR6 unique built-in dual image storage tailored to OTA reprogramming needs and provide high speed security cryptographic services, for instance for network authentication.

Table 1. SR6P6x overview

Feature		SR6P6x
Cortex®-R52+ cores (+ checker cores)		6 cores (+4 checkers), configurable as 5 cores (+5 checkers)
NEON (with SIMD, dual precision floating point)		No
Cache (instruction / data) per core in Kbyte		32 / 32
Core memory protection unit (regions), several additional protection mechanisms in the architecture, for example: NOC firewalls	Hypervisor (EL2)	24
	OS (EL1)	24
Code NVM	Overall including HSM in Mbyte	16
	Cluster code NVM in Mbyte	15.5
	HSM code NVM in Kbyte	512
Code NVM built-in memory replication for OTA reprogramming (not supported by HSM) in Mbyte		Up to 2x 15.5
Data NVM in Kbyte		640
RAM in Kbyte		2304
Hardware security module (HSM) - 2nd generation		Yes
AES-Light (cryptographic services - in lockstep)		4
Arm® Cortex®-M4	Multi-purpose accelerator (DSPH)	1
	Multi-purpose accelerator in lockstep (DME)	1
Stand-by and smart power modes		No
eDMA engines (number of channels, more channels through muxes/channel)	Engine	4
	Channel	3 x 32 1 x 64
LIN and UART (LINFlexD)		11
CAN-FD		12

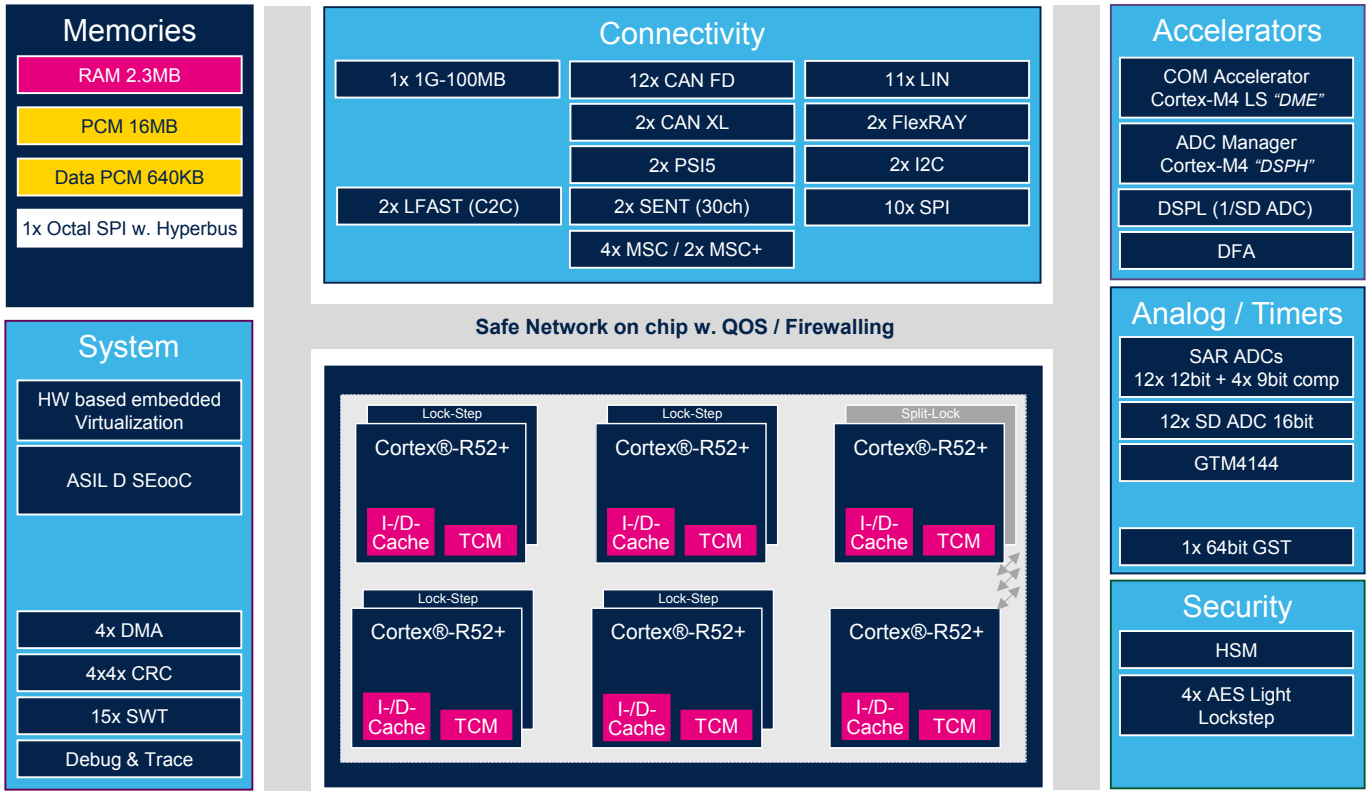
Feature		SR6P6x
CAN-XL		2
SPIQ (with LVDS channel)		10 (2)
Microsecond channel (MSC)		4
Microsecond channel plus (MSCP)		2
SENT	Unit	2
	Channel/unit	15
I^2C		2
PSI5	Unit	2
	Channel/unit	1 channel
FlexRay (dual channel)		2
Gigabit ethernet IEEE 802.3-2008 compliant (with MII, RMII, RGMII)		1
SIPI / LFAST interprocessor bus		2
Generic timer modules (GTM4)	GTM4144	1
High-resolution timer		No
12-bit SAR analog converters		12
16-bit sigma-delta analog converters (units with DSPL)		12 (12)
9-bit SAR analog comparators		8
OctalSPI (support HyperBus™ memory devices)		Yes
SDMMC interface		No
Debug port	Main debug port (JTAG+SWD)	Yes
	Secondary debug port (SWD)	Yes
High speed off-chip trace lane (multi GBit/s protocol)		0 (on production device) 4 (on family emulation device)
Max temperature (target)	Junction temperature	165 °C(1)
Packages	FPBGA 516	X
	FPBGA 292	X

1. *Nominal specification up to 150 °C. Delta specification up to 165 °C.*

1.3 Block diagram

The figure below shows the top-level block diagram.

Figure 1. Block diagram



Revision history

Table 2. **Document revision history**

Date	Version	Changes
29-Jun-2020	1	Initial ST Restricted release.
26-Apr-2021	2	Second ST Restricted release.
15-Jun-2022	3	Initial public release.
24-Jun-2022	4	• In the whole document: replaced Cortex®-R52 by Cortex®-R52+ • Peripheral, IOs, communication interfaces: updated the bullet: "Interconnection with GTM..."

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