A High Power Factor Flyback with Constant-Current Output for LED Lighting Applications

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Abstract — This article explains the principles of AC/DC converters in flyback topology having a high power factor input and a constant current output. The most commonly used mode of operation for this purpose is boundary conduction mode (BCM). The basics of this mode are developed and its drawbacks are made clear. A simple method for improving power factor is introduced and explained in detail. Operating in DCM mode improves power factor and THD while reducing the peak drain voltage. A quick design example is given and the special issues of driving high power LEDs are explained.

I. INTRODUCTION

Due to their long lifetime and excellent efficacy, high-power LEDs are increasingly used in general lighting applications. Two things are important when driving LEDs: they must be operated with constant current and the ballast must have a high power factor. While international standards dictate power factor correction mandatory for input powers above 25W, the new Energy-Star directive for solid-state lighting requires a power factor greater than 0.9 for power levels above 3W.

While it is possible to achieve this by passive power factor correction (PFC), it is desirable to have a cost-effective solution that can achieve even better performance with low weight and small form factor. A flyback converter with low harmonic content input current is one possible solution.

II. HIGH POWER FACTOR FLYBACK: BASICS OF OPERATION

The basic idea behind the high power factor (PF) flyback is to control it using a boundary conduction mode (BCM) PFC controller like the FAN7527B. The FAN7527B forces the peak drain current to follow the shape of the input voltage similar to a PFC pre-regulator in boost topology but with some differences in operation.

First, the bulk capacitor after the rectifier is removed which is the primary reason for poor power factor of the switch-mode power supply (SMPS). This is because it only allows input current flow when the input voltage is higher than the voltage of the bulk capacitor which is essentially constant. Thus, the input current of a SMPS with a bulk capacitor consists of short and high peaks having high harmonic content and higher RMS and peak values than a sinusoidal current would have at same output power. In contrast, the value of C1 in the simplified schematic (Fig. 1) is only a few hundreds of a nF and this cap acts as a high frequency filter only. Obviously, the flyback following this input stage is not supplied by a DC voltage but by half-waves with double the line frequency.

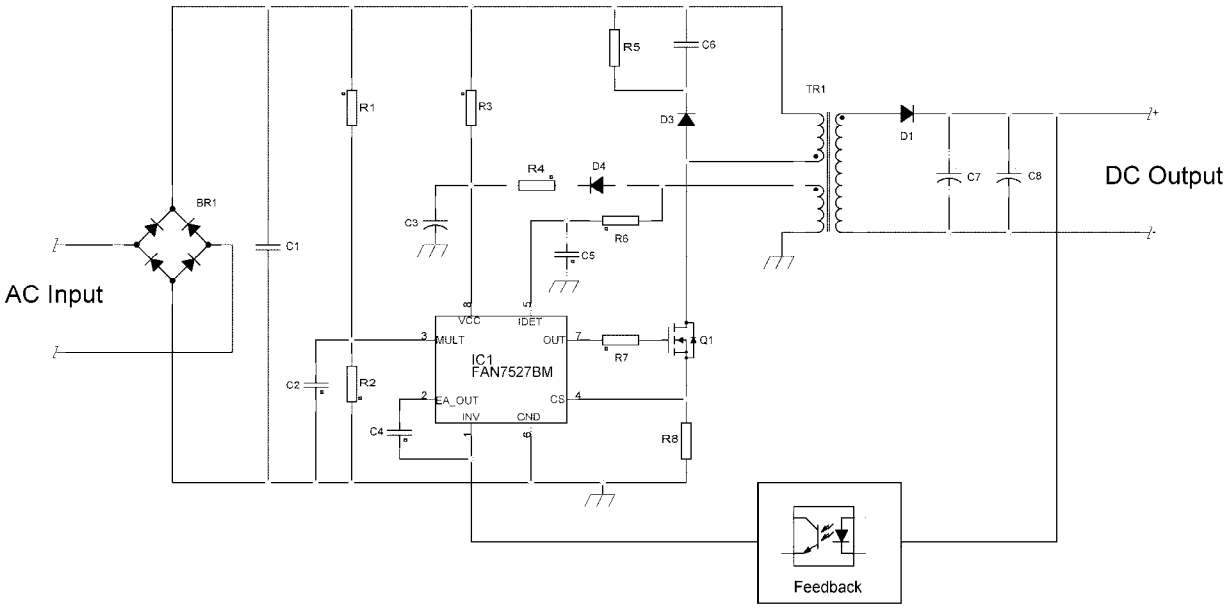

Fig. 1: Simplified schematic of high-power flyback operating in BCM.

The basic operation of the flyback is as follows: When MOSFET Q1 is turned on, the current in the primary side of the transformer increases linearly. The current through Q1 is sensed with R8 and the corresponding voltage is fed to the sense pin 'CS' of the controller. An internal comparator turns the MOSFET off as soon as the sense pin reaches a level that is determined by the voltage at the pin 'MULT' and the output of the error amplifier. To allow a good power factor, the error amplifier output must be nearly constant during one half–cycle of the input voltage. Thus, the shape of the peak drain current is determined by the voltage at the 'MULT' input, which is the rectified and scaled down input voltage. Consequently, if the input voltage is sinusoidal, the envelope of the primary side peak drain current is sinusoidal as well.

Since both the rate of change of the inductor current and the peak inductor current are proportional to the instantaneous input voltage, the on-time is constant

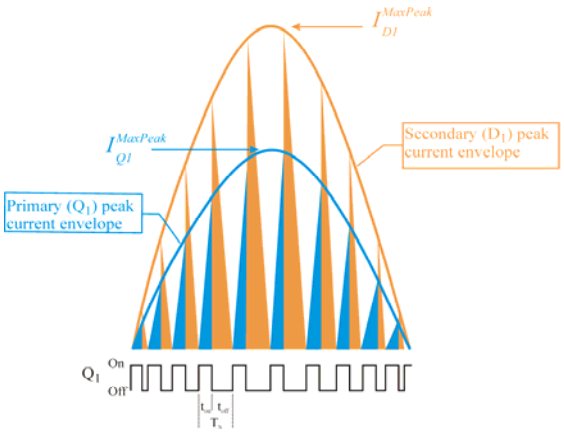

Fig. 2: Timing and currents in BCM flyback.

over the complete half-cycle.

When the MOSFET is turned off, the input current instantly drops to zero, unlike the boost converter where it goes down linearly. As in any flyback the secondary side diode now conducts and the energy stored in the magnetic field is transferred to the output. The diode current decreases linearly, starting from a value that is n times higher than the primary side peak, with n being the transformer turns primary to secondary turns ratio. The diode current drops at a constant rate while the peak value is proportional to the momentary input voltage. This leads to a variable time until the current falls to zero and the next switching cycle is initiated. Together with the constant on-time, the variable off-time results in a variable switching frequency.

To determine the actual shape of the input current, the average value of the transformer current has to be determined; in the real application, the EMI filter will do that for you. For this purpose, the momentary switching frequency and duty cycle are needed.

First, the on-time of Q1 is calculated (Θ is defined as $2\cdot\pi\cdot f_L\cdot t$ with f_L being the line frequency):

$$t_{On} = \frac{L_P \cdot I_{Q1}^{Peak} \cdot |\sin(\Theta)|}{V_{In}^{Peak} \cdot |\sin(\Theta)|} = \frac{L_P \cdot I_{Q1}^{Peak}}{V_{In}^{Peak}} \qquad (1)$$

This formula confirms that t_{On} is constant over a half-cycle. The off-time is given by:

$$\begin{aligned} t_{Off} &= \frac{L_S \cdot I_{D1}^{Peak} \cdot |\sin(\Theta)|}{V_{Out} + V_{D1}^{Fwd}} \\ &= \frac{\frac{L_P}{n^2} \cdot n \cdot I_{Q1}^{Peak} \cdot |\sin(\Theta)|}{V_{Out} + V_{D1}^{Fwd}} \end{aligned} \qquad (2)$$

As expected, the off-time varies over the half-cycle. Together, equations (1) and (2) give the switching period, T_S:

$$\begin{aligned} T_S &= \frac{L_P \cdot I_{Q1}^{Peak}}{V_{In}^{Peak}} + \frac{L_P \cdot I_{Q1}^{Peak} \cdot |\sin(\Theta)|}{n \cdot (V_{Out} + V_{D1}^{Fwd})} \\ &= \frac{L_P \cdot I_{Q1}^{Peak}}{V_{In}^{Peak}} \left(\frac{n \cdot (V_{Out} + V_{D1}^{Fwd}) + V_{In}^{Peak} \cdot |\sin(\Theta)|}{n \cdot (V_{Out} + V_{D1}^{Fwd})} \right) \end{aligned} \qquad (3)$$

One important design parameter for flyback topology is the reflected voltage $V_R = n \cdot (V_{Out} + V_{D1}^{Fwd})$, which is the voltage that occurs across the primary side of the transformer while the secondary diode is conducting. A higher V_R value increases the voltage stress on the MOSFET drain. Because of this, there is the general tendency to keep V_R small. The switching frequency is derived from Equation (3), resulting in a simpler formula:

$$f_S = \frac{V_{In}^{Peak}}{L_P \cdot I_{Q1}^{Peak}} \left(1 + \frac{V_{In}^{Peak}}{V_R} \cdot |\sin(\Theta)| \right)^{-1} \qquad (4)$$

From this formula, the minimum switching frequency always occurs at the line voltage maximum, while the maximum frequency is reached at the line zero crossing. One important design parameter is missing: duty-cycle d, given by the equation:

$$d = \frac{1}{1 + \frac{V_{In}^{Peak}}{V_R} \cdot |\sin(\Theta)|} \qquad (5)$$

and varies over the line cycle in the same way the switching frequency does.

The next issue is to determine whether the input current will be sinusoidal (as was originally intended). Only the expression for the variation of the peak MOSFET current with time, or better to say with phase angle, has to be determined. Bearing in mind that this peak value is forced to follow the shape of the input voltage (Fig. 2), this equation can be expressed as follows:

$$I_{Q1}^{Peak}(\Theta) = I_{Q1}^{MaxPeak}\left|\sin(\Theta)\right| \qquad (6)$$

The current averaged over one switching cycle is then given by the area of the triangular drain current times the momentary duty cycle:

$$I_{In}(\Theta) = \frac{1}{2}\cdot I_{Q1}^{MaxPeak}\cdot\left|\sin(\Theta)\right|\cdot d$$

$$= I_{Q1}^{MaxPeak}\cdot\frac{\left|\sin(\Theta)\right|}{2\cdot\left(1+\frac{V_{In}^{Peak}}{V_R}\cdot\left|\sin(\Theta)\right|\right)}. \qquad (7)$$

The result of (7) is quite disappointing since the denominator makes the current shape clearly non-sinusoidal, unless the ratio $R_{VR} = \frac{V_{In}^{Peak}}{V_R}$ is made very small. It is clearly visible from Fig. 3 that for RV > 1, the current is not sinusoidal.

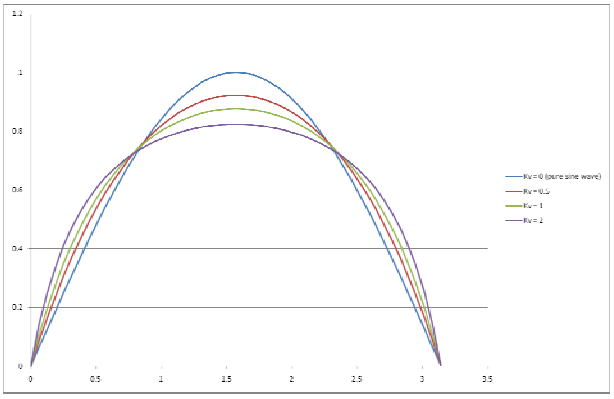

Fig. 3: Shape of the input current of BCM flyback with R_{VR} as an parameter.

Note that the reflected voltage, V_R, adds to the input voltage during the off-time of the MOSFET. Making the ratio small, such as 0.1, would result in a drain voltage which is more than eleven times the input voltage. Such a high reflected voltage is impossible to handle even if the input voltage is only $110V_{RMS}$. Feasible values for R_{VR} are in the range of 1 for US and 2 to 3 for European input voltage. Harmonic analysis of the input current shape shows that it is difficult to get a THD lower than 10%, mandatory for lighting equipment above 25W, with a R_{VR} of 2. Hence, the described application is more suited for US input voltages. For European applications, an 800V or even an 1000V MOSFET must be used to comply with the regulations for lighting equipment. Nevertheless, the power factor itself is still in the range of 0.95 when R_{VR} is 2 and the BCM flyback method for PFC is usable for many applications that need a relatively high PF but not a low THD.

A careful review of the equations above lead to the following conclusions:

1. The input voltage as a reference for the MOSFET peak drain current is not needed. If the on-time is made constant over one half-cycle, the peak drain current will follow the input voltage.
2. The main reason for the non-ideal shape of the input current is the variable frequency or rather the variable duty-cycle. With the identical drain current shape, if the duty-cycle were kept constant over a half-cycle, the input current would be sinusoidal.

Obviously these two things can be accomplished with a "traditional" PWM controller. This implementation is most easy if a voltage mode (VM) controller is used. If the feedback loop is slow enough, the duty cycle will be constant i.e. the desired constant on-time is achieved. Unfortunately it is difficult to find a state of the art voltage mode controller for offline applications on the market since current mode devices have so many advantages for standard off-line applications. A possible choice is the KA7552A or KA7553A which differ only in the maximum duty-cycle.

If a current mode (CM) controller is used, the peak current has to be set to be proportional to the input voltage as implemented in current mode PFC controllers. But these devices are all designed for BCM and must be driven by an external oscillator to operate with constant f_S. Hence, the voltage mode PWM controller seems to be a smart choice.

As will be shown later, it is possible to turn the BCM controllers FAN7527 (CM), FAN7529/30 (VM), FAN6961 (VM), and similar into constant frequency controllers with a few inexpensive external components.

III. HIGH POWER FACTOR FLYBACK WITH CONSTANT F_S AND DUTY-CYCLE

The main advantage of this approach is that an excellent power factor and THD can be achieved regardless of the V_R choice. As in the "traditional" flyback, a lower V_R leads to higher peak and RMS current through the MOSFET and the designer can select for optimum balance. The main point is to guarantee that the flyback operates in DCM over the whole half-cycle with some margin. That means that the application works close to BCM at the maximum of the input waveform. A simplified schematic with the KA7552 controller is shown in Fig. 5.

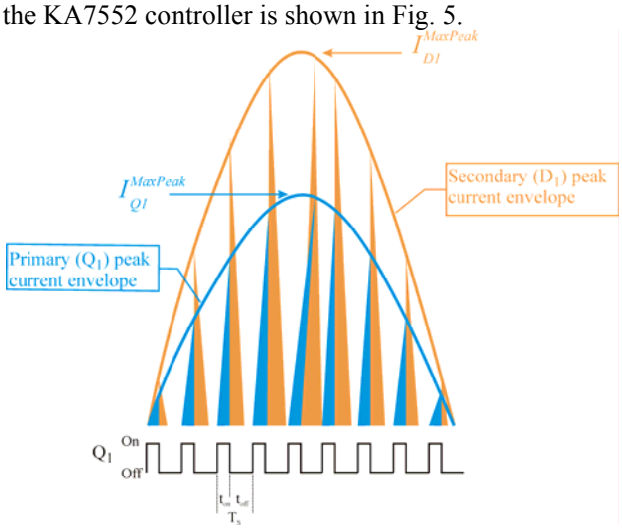

Fig. 4:Timing and currents in DCM flyback.

The switching frequency is determined by R2 and C2 while C4 determines the soft start time and R7 the maximum MOSFET current.

The important design parameters can be determined in a similar manner to that for the BCM flyback with the difference that the duty cycle and frequency are constant over a line half-wave.

The MOSFET peak current can be calculated from the input power:

$$\begin{aligned} P_{In} &= \overline{V_{In}(\Theta) I_{In}(\Theta)} \\ &= \frac{1}{\pi}\int_0^{\pi}\left(V_{In}^{Peak}\cdot|\sin(\Theta)|\cdot\frac{I_{Q1}^{MaxPeak}}{2}\cdot|\sin(\Theta)|\cdot d\right)d\Theta \\ &= \frac{I_{Q1}^{MaxPeak}\cdot V_{In}^{Peak}\cdot d}{2\pi}\int_0^{\pi}\sin(\Theta)^2\,d\Theta \\ \Rightarrow\quad I_{Q1}^{MaxPeak} &= \frac{4\cdot P_{In}}{V_{In}^{Peak}\cdot d} \end{aligned} \tag{8}$$

It is not surprising that the maximum peak drain current comes out to be twice the value of that in a DC supplied flyback of the same power.

To calculate the conduction loss of the switch the RMS-value of the primary current is determined by considering the RMS-value of each triangle of $I_{Q1}(\Theta)$ and then averaging over a line half-cycle:

$$\begin{aligned} I_{Q1}^{RMS} &= \sqrt{\frac{d}{3\pi}\int_0^{\pi}\left(I_{Q1}^{MaxPeak}\cdot|\sin(\Theta)|\right)^2 d\Theta} \\ &= I_{Q1}^{MaxPeak}\cdot\sqrt{\frac{d}{6}} \end{aligned} \tag{9}$$

Having the peak and RMS switch current, Q_1 can be selected easily. Although both currents are higher than in a DC supplied flyback, they are almost identical or even lower than those of a BCM flyback with a $R_{VR} \approx 1$. For both the BCM and DCM flybacks, the RMS currents can be reduced by increasing the duty cycle, at the expense of increasing peak drain voltage.

The duty cycle not only affects the switch currents but is important for the transformer design as well. Since the circuit has to operate in DCM under all conditions, the primary side inductance has to be chosen according to the formula:

$$L_P \le \frac{U_{In}^{Peak}\cdot t_{On}}{I_{Q1}^{MaxPeak}} = \frac{\left(U_{In}^{Peak}\cdot d\right)^2}{4\cdot P_{In}\cdot f_S} \tag{10}$$

where f_S is the switching frequency. To stay in DCM the secondary side current must fall to zero during the off-time of the switch leading to the equation:

$$\begin{aligned} t_{Off} &= \frac{1-d}{f_S} \ge \frac{L_S\cdot I_{D1}^{MaxPeak}}{V_{Out}+V_{D1}^{Fwd}} = \frac{L_P\cdot I_{Q1}^{MaxPeak}}{n\cdot\left(V_{Out}+V_{D1}^{Fwd}\right)} \\ \Rightarrow\quad n &\ge \frac{L_P\cdot I_{Q1}^{MaxPeak}\cdot f_S}{(1-d)\cdot\left(V_{Out}+V_{D1}^{Fwd}\right)} \ge \frac{d}{(1-d)}\frac{U_{In}^{Peak}}{\left(V_{Out}+V_{D1}^{Fwd}\right)} \end{aligned} \tag{11}$$

Nevertheless, an alternative and more often used approach is to select the reflected voltage V_R since the latter determines, together with the maximum input voltage and the voltage across the clamping network ΔV, the maximum drain voltage. In this case the duty cycle has to be:

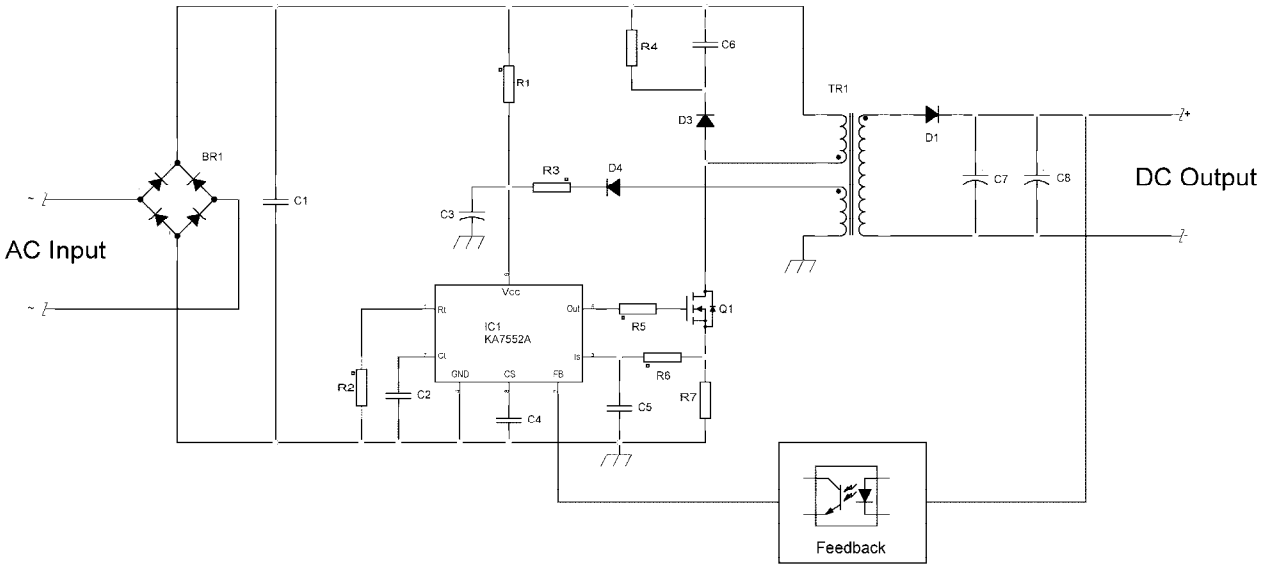

Fig. 5: Simplified schematic of high power flyback operating in DCM.

$$d \le \frac{V_R}{U_{In}^{Peak} + V_R} \tag{12}$$

Since the maximum d occurs at minimum input voltage, the latter has to be used when determining the duty cycle.

To calculate the transformer turns, the secondary side RMS current and a suitable transformer core size need to be determined.

The secondary current can be calculated from the maximum peak diode current, that is n times the maximum peak switch current, and the duty cycle of the diode current, that varies over the line half cycle.

The duty cycle of D1 is given by:

$$d_{D1} = t_{D1}^{Conduct}(\Theta) \cdot \mathrm{f_S} = \frac{\mathrm{L_P} \cdot I_{Q1}^{MaxPeak} \cdot \left|\sin(\Theta)\right| \cdot \mathrm{f_S}}{\mathrm{V_R}} \tag{13}$$

and the RMS current is determined in a similar manner as the switch RMS current:

$$\begin{aligned} \mathrm{I}_{D1}^{RMS} &= \sqrt{\frac{L_P \cdot f_S \cdot \left(I_{D1}^{MaxPeak}\right)^2 \cdot I_{Q1}^{MaxPeak}}{3 \cdot V_R \cdot \pi} \int_0^{\pi} \left|\sin(\Theta)\right|^3 d\Theta} \\ &= I_{D1}^{MaxPeak} \cdot \sqrt{\frac{4 \cdot L_P \cdot f_S \cdot I_{Q1}^{MaxPeak}}{9 \cdot \pi \cdot V_R}} \end{aligned} \tag{14}$$

If in equations (10) and (11) or (12), the inequalities are turned to equations, this simplifies to:

$$\mathrm{I}_{D1}^{RMS} = n \cdot I_{Q1}^{MaxPeak} \cdot \sqrt{\frac{4 \cdot (1 - \mathrm{d})}{9 \cdot \pi}} \tag{15}$$

A helpful formula to estimate the core size is:

$$A_e \cdot A_w \ge 2 \left(\frac{L_P \cdot I_{Q1}^{RMS} \cdot I_{Q1}^{PeakMax} \cdot 10^4}{90 \cdot B_{Sat}} \right)^{1.31} \tag{16}$$

When L_p is given in H, current in A, and flux density in T, the result will be in cm^4. The saturation flux density can be chosen to be 0.35T in this application even when the switching frequency is as high as 100 kHz. The reason is that this relative high flux density will only occur in the line voltage maximum; the average as well as the RMS flux density is much lower. The factor of two in (16) has to be introduced since the 'usage' of the transformer is not as good as in a normal flyback: around the line zero crossing, very little energy can be transferred resulting in the need for more energy transfer around the maximum of the line voltage.

When a value for L_P and the transformer core have been chosen, the number of primary turns can be calculated with the well known formula:

$$N_P \ge \frac{L_P \cdot I_{Q1}^{PeakMax}}{A_e \cdot B_{Sat}} \tag{17}$$

Finally the clamp network design is similar to that of the standard flyback, though the power dissipation is different:

$$\begin{aligned} P_{SN} &= \frac{1}{\pi} \int_0^{\pi} \left(\frac{1}{2} \cdot f_S \cdot L_{Leak} \cdot I_{Q1}^{Peak}(\Theta)^2 \frac{V_{SN}}{V_{SN} - V_R} \right) d\Theta \\ &= \frac{1}{4} \cdot f_S \cdot L_{Leak} \cdot I_{Q1}^{MaxPeak\,2} \frac{V_{SN}}{V_{SN} - V_R} \end{aligned} \tag{18}$$

In the equation above it has been assumed that the voltage of the capacitor of the clamping network is constant. For moderate capacitor values it will actually vary over the half cycle. Equation 18 gives an upper level for the dissipation of the network. The value of the clamp resistor value is then given by:

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} = \frac{4 \cdot V_{SN} \cdot (V_{SN} - V_R)}{f_S \cdot L_{Leak} \cdot I_{Q1}^{MaxPeak\,2}} \quad (19)$$

In both types of high PF Flyback, BCM, and DCM, the energy transferred to the secondary is modulated by sin(Θ)2 resulting in a relative strong modulation of the output voltage. Thus, the output capacitors must have a high value compared to the standard flyback. The value of the output cap should be chosen to be:

$$C_O \geq \frac{I_{Out}^{Max}}{2 \cdot \pi \cdot f_L \cdot \Delta V_{Out}} \quad (20)$$

IV. DESIGN EXAMPLE

A quick design example for a high power factor flyback is described below.

A. *Design Specifications:*

- Mains voltage range: V_{ACmin} = 185 V_{AC}, V_{ACmax} = 265 V_{AC}
- Mains frequency: f_L = 50 Hz
- DC Output Voltage: V_{Out} = 48 V
- Output current: I_{Out} = 0.7 A
- Maximum $2f_L$ output ripple: ΔV_o = 1 V_{PP}

B. *Pre-Design Choices:*

- Switching frequency: f_S = 70 kHz
- Reflected voltage: V_R = 100V
- Overvoltage due to leakage inductance: ΔV =50V (half the reflected voltage is a typical value)
- Expected efficiency: η = 80%

With the above choice of reflected voltage and overvoltage due to leakage inductance the maximum drain voltage will be:

$$V_{Q1}^{Dsmax} = V_{ACmax} + V_R + \Delta V$$
$$= 265V \cdot \sqrt{2} + 100V + 50V$$
$$= 524.76V$$

This implies that a 600V MOSFET can be used with some spare margin.

C. *Design Steps*

a. Calculate the total expected input power:

$$P_{In} = \frac{P_{Out}}{\eta} = \frac{48V \cdot 0.7A}{0.8} = 42W$$

b. Since V_R has been selected as 100V, determine d:

$$d = \frac{V_R}{U_{In}^{Peak} + V_R} = \frac{100}{185V \cdot \sqrt{2} + 100} = 0.277$$

c. Now we get the peak and RMS current for the MOSFET and primary side of the transformer. Input rectifier and MOSFET forward loss are neglected here.

$$I_{Q1}^{MaxPeak} = \frac{4 \cdot P_{In}}{V_{ACmin}^{Peak} \cdot d} = \frac{4 \cdot 42W}{185V \cdot \sqrt{2} \cdot 0.277}$$
$$= 2.322A$$
$$I_{Q1}^{RMS} = I_{Q1}^{MaxPeak} \cdot \sqrt{\frac{d}{6}} = 0.499A$$

d. Determine the maximum value for the primary side inductance:

$$L_P = \frac{(U_{In}^{Peak} \cdot d)^2}{4 \cdot P_{In} \cdot f_S} = \frac{(185V \cdot \sqrt{2} \cdot 0.277)^2}{4 \cdot 42W \cdot 70kHz}$$
$$= 446\mu H$$

e. Find the right transformer core:

$$A_e \cdot A_w \geq 2\left(\frac{L_P \cdot I_{Q1}^{RMS} \cdot I_{Q1}^{PeakMax} \cdot 10^4}{90 \cdot B_{Sat}}\right)^{1.31}$$
$$= 2\left(\frac{446\mu H \cdot 0.499A \cdot 2.322A \cdot 10^4}{90 \cdot 0.35T}\right)^{1.31}$$ While the
$$\approx 1873mm^4$$

EF20 core has a core product of only 1088 mm^4 typical, the EF25 has 3224 mm^4 and should be sufficient for this application.

f. The minimum number of primary turns will be:

$$N_P \geq \frac{L_P \cdot I_{Q1}^{PeakMax}}{A_e \cdot B_{Sat}} = \frac{446\mu H \cdot 2.322A}{52 \cdot 10^{-6} m^2 \cdot 0.35T}$$
$$= 59.9\,Turns$$

g. The turns ratio is determined by the selection of the reflected Voltage V_R:

$$n = \frac{V_R}{V_{Out} + V_{D1}^{Fwd}} = \frac{100V}{48V + 1V}$$
$$= 2.0408$$

h. Finally the secondary side current is needed:

$$I_{D1}^{RMS} = n \cdot I_{Q1}^{MaxPeak} \cdot \sqrt{\frac{4 \cdot (1 - d)}{9 \cdot \pi}}$$
$$= 2.0408 \cdot 2.322A \cdot \sqrt{\frac{4 \cdot 0.723}{9 \cdot \pi}}$$
$$= 1.516A$$

Real turn numbers and wire diameters can now be determined in the same way as for a standard flyback. The same is true for the MOSFET and diode voltage stress.

i. The resistor of the clamp network can be selected with the assumption that the leakage inductance is 2.5% of the primary side inductance. The latter value depends on the construction of the transformer and may be higher for bigger and lower for smaller transformers:

$$R_{SN} = \frac{4 \cdot V_{SN} \cdot (V_{SN} - V_R)}{f_S \cdot L_{Leak} \cdot I_{Q1}^{MaxPeak\,2}}$$
$$= \frac{4 \cdot 150V \cdot 50V}{70kHz \cdot 11.2\mu H \cdot 2.322A^2}$$
$$= 7097.1\Omega$$
$$P_{SN} = \frac{1}{4} \cdot f_S \cdot L_{Leak} \cdot I_{Q1}^{MaxPeak\,2} \frac{V_{SN}}{V_{SN} - V_R}$$
$$= \frac{70kHz \cdot 11.2\mu H \cdot 2.322A^2 \cdot 150V}{4 \cdot 50V}$$
$$= 3.17W$$

A 6.8kΩ / 5W resistor should be selected as initial choice. The value has to be adjusted with the real design.

j. If the ripple shall be limited to 0.5V the output caps must be at least:

$$C_O \geq \frac{I_{Out}^{Max}}{2 \cdot \pi \cdot f_L \cdot \Delta V_{Out}} = \frac{0.7A}{314.159s^{-1} \cdot 0.5V}$$
$$= 4.45mF$$

Normally such big caps can deal with the superimposed high frequency ripple without the need for low ESR / high ripple current types.

V. DRIVING THE LED

A LED is a semiconductor diode that is operated in the forward direction and may emit electromagnetic radiation in the range from IR to UV. While a LED normally is made from compound semiconductors like GaAs or GaP, it shows an I-V characteristic similar to a standard silicon diode. Only the forward voltage, V_F, is considerably higher with up to 4.5V for a white high power LED.

The steep V_{Fwd}-I_{Fwd} characteristic of a diode is one reason why a LED can't be driven by a voltage source. Consider a white OSRAM® 'Platinum DRAGON®', LW-W5SN as an example. At the specified operating point of I_{Fwd} = 700mA, the typical forward voltage is 3.6V and the current varies by about 100mA when the voltage is changed by 100mV. This would not be a problem by itself since it is not an issue to stabilize a voltage to, say, ±1%. This would be ±36mV in this specific case and the resulting change in current would be around ±36mA. Since brightness and color of a LED are primarily determined by I_F, this would lead to an acceptable change in brightness of around ±5%. But there are two additional parameters that make voltage drive an unfeasible approach. First, the forward voltage may vary over a wide range depending on production parameters. For the above mentioned LED, V_{Fwd} ranges from 2.9V to 4.3V and very careful V_F selection would be necessary if voltage drive was intended. Finally, the large temperature coefficient of -3.. -6 mV/K makes a stable voltage driven operation impossible, even with selected V_F.

The classical approach for stable operation of a LED is to stabilize current with a series resistor. For a high power LED, this resistor would dissipate too much power, thus leading to additional thermal problems and, most important, messing up the efficacy of the LED.

Consider the mentioned LED with a V_F variation ΔV_{Fwd} of ±700mV at 25C and select a series resistor, R, that keeps the diode current within 5% of the rated current.

Two LEDs with forward voltages differing by ΔV_{Fwd} would have two respective currents:

$$I_1 = \frac{V_{In} - V_{Fwd}}{R_{Ser}} \quad (21)$$

and

$$I_2 = \frac{V_{In} - (V_{Fwd} + \Delta V_{Fwd})}{R_{ser}} \quad (22)$$

The difference is:

$$\Delta I_{Fwd} = \frac{\Delta V_{Fwd}}{R_{Ser}}. \quad (23)$$

If the latter variation is limited to ±10% of the nominal value,

$$\frac{\Delta V_{Fwd}}{R_{Ser}} \leq 0.1 \cdot \frac{V_{In} - V_{Fwd}}{R_{ser}} \quad (24)$$

then the following relation for the drop across the stabilization resistor is:

$$V_{In} - V_{Fwd} \geq 10 \cdot \Delta V_{Fwd}. \quad (25)$$

The drop across the resistor must be ten times the variation in forward voltage which would be 7V in this example. That would result in a power dissipation of 4.9W in the resistor, more than the LED itself.

If it was not because of the poor efficiency, thermal considerations would rule out this solution. Since the LED is a semiconductor device, its temperature must be kept as low as possible. A major effort when designing LED based luminaries is good thermal design. A resistor dissipating such an amount of additional heat is not desirable and seems, even with a more relaxed specification, not the best approach. The proper approach to drive LEDs is a constant current source with the LEDs connected in series.

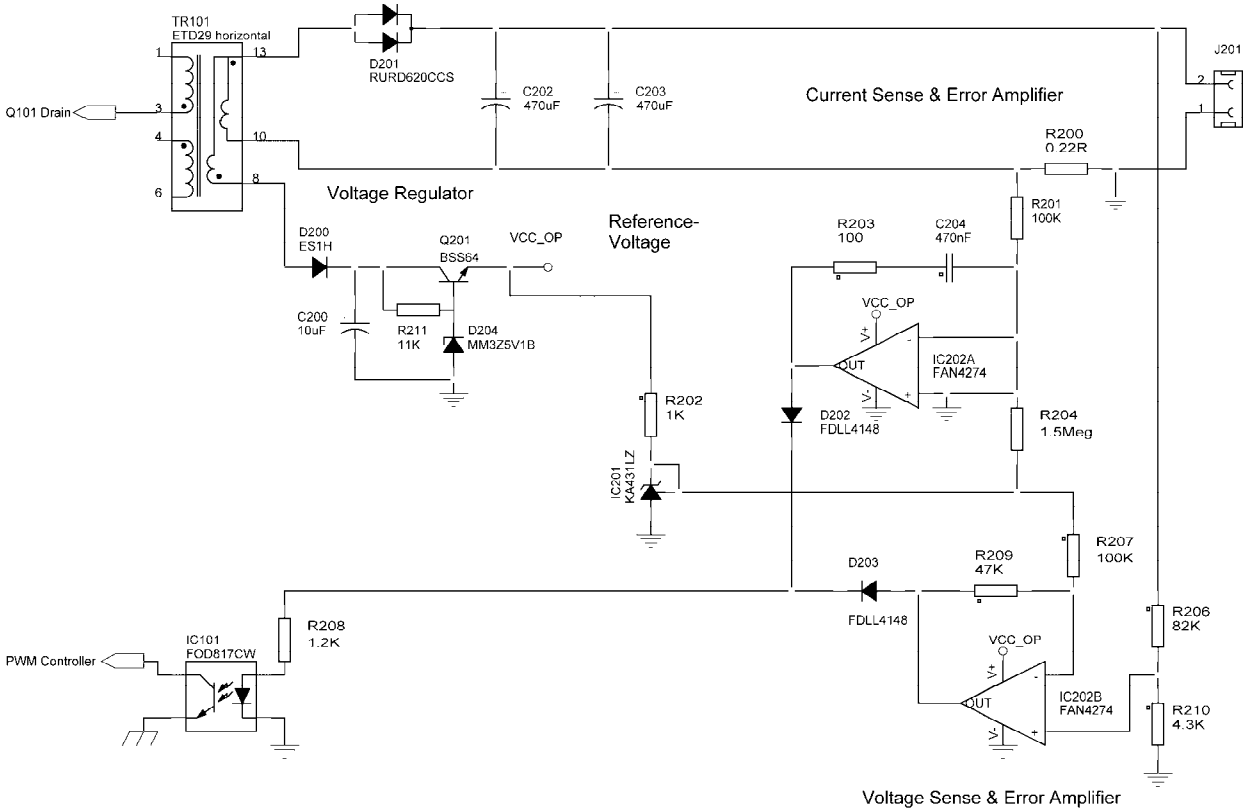

Fig. 6: Feedback loop.

VI. CONSTANT CURRENT OUTPUT

The constant current output is implemented by measuring the actual output current with the help of a sense resistor and generating a suitable feedback signal to control the duty cycle of the PWM controller. The feedback loop consists of two different paths designed around the dual RRIO operational amplifier FAN4274. The voltage feedback loop is made from one half of this device and the current feedback from the other.

Since the FAN4274 has no built-in reference voltage, the latter is implemented with the precision shunt regulator, KA431 (IC201), and the series resistor R202. When the cathode is connected to the reference input, the reference voltage, V_{Ref}, at the node R204/R207 is 2.5V.

As long as there is no output current, the voltage drop across the shunt R_{200} is 0V. Hence, the potential at the inverting input of IC202A is:

$$V_{IC202A}^{Inv} = V_{R200} + (V_{Ref} - V_{R200}) \cdot \frac{R_{201}}{R_{201} + R_{204}} = 0V + 2.5V \cdot \frac{2.1}{35.1} = 0.15V \quad (26)$$

Since the non-inverting input of IC_{202A} is connected to ground, its output will have the potential of the negative supply rail, which is ground in this case. Consequently, no current will flow through D_{202}. In this case, the current loop is inactive.

When there is output current, the node R_{200}/R_{201} goes negative to ground and the voltage at the inverting input of IC_{202A} drops as well. If the offset voltage of the OPAMP is neglected, the output will go positive as soon as the inverting input has crossed 0V.

The latter happens when the voltage across R200 reaches:

$$V_{R200} = V_{Ref} \cdot \frac{R_{201}}{R_{204}} = 2.5V \cdot \frac{2.1}{33} = 0.159V \quad (27)$$

Now the output voltage of IC202A will be positive, driving current through D202 and the LED of the optocoupler and reducing the duty cycle of the FAN7527B. The actual set-point of the output can be determined as:

$$I_{Out} = \frac{V_{Ref} \cdot R_{201}}{R_{204} \cdot R_{204}} = \frac{2.5V \cdot 2.1k\Omega}{33k\Omega \cdot 0.22\Omega} = 0.723A \quad (28)$$

The voltage loop works in a similar manner. The inverting input of IC202B is connected to the 2.5V reference via R207. The output of this amplifier stays low as long as the voltage at the non-inverting input:

$$V_{IC202B}^{Non\ Inv} = V_{Out} \cdot \frac{R_{210}}{R_{210} + R_{206}} = V_{Out} \cdot 0.05213 \qquad (29)$$

is lower than 2.5V and rises if this value is exceeded. It is easy to obtain the maximum output voltage:

$$V_{Out} = \frac{V_{Ref}}{0.05213} = 48V \qquad (30)$$

As long as the output current is lower than 0.723A, the voltage loop will keep the output voltage at 48V. In this case, the output of IC_{202A} is low with D_{202} preventing any current flow i.e. the voltage loop is active and the current loop is inactive. If the output current exceeds the set-point, the output of IC_{202A} drives additional current through the LED of the optocoupler, resulting in a lower duty-cycle and in turn, lower output voltage. This results in output of IC_{202B} dropping to zero. Now D_{203} prevents current flow and the current loop is active.

The operational amplifier and the reference voltage are supplied by a simple linear regulator that is implemented with the components Q200, R211, and D204. The reason for using an additional regulator is quite simple: the output voltage of the ballast may vary from about 3V to 48V i.e. by a factor of 16. The same is true for the transformer winding generating the supply voltage for the operational amplifier. If a minimum supply voltage of 4.5V is assumed, the maximum would be around 75V. Consequently an additional regulator with about 80V maximum input voltage is needed.

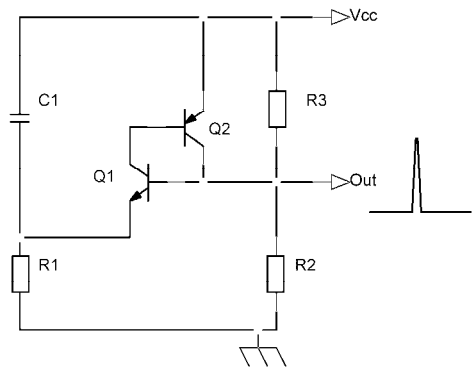

Fig. 7: Simple oscillator with two transistor PUT

The feedback level at the control input of the PWM has to be constant over a line half-cycle. The output on the other hand has a considerable 100Hz ripple. If the feedback loop tried to eliminate this ripple, that would result in a control signal trying to draw more current around the zero crossing of the line and less around the maximum i.e. decrease the power factor. In order to prevent this from happening, the bandwidth has to be set to a very low value with C204.

The low loop bandwidth is not a problem under normal operating conditions since the LED is not a very dynamic load. Nevertheless, at startup, overshoots may occur especially if the number of LEDs connected is small.

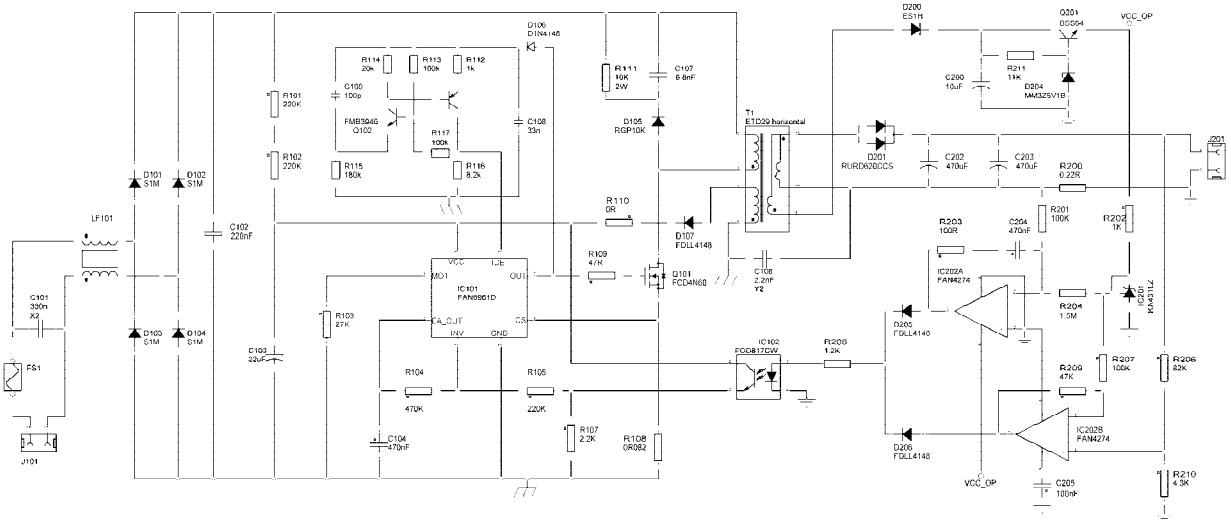

Fig. 8: Complete schematic of high power factor flyback in DCM mode.

VII. USING BCM CONTROLLERS WITH CONSTANT SWITCHING FREQUENCY

As mentioned earlier, it is possible to operate the BCM controllers e.g. FAN7527 with constant switching frequency by adding a simple oscillator. The oscillator should be inexpensive but nevertheless have good performance in terms of stability and power consumption. Unless the added oscillator has its own supply voltage supervisor, it can not be connected directly to the V_{CC} of the BCM controller because it might start drawing current before the controller does and thus adversely affect the startup sequence.

Since the oscillator does not have to be one with a square-wave but needs to deliver short sync pulses, a very simple circuit with a programmable unijunction transistor (PUT) has been chosen. The latter can be easily replaced with the well known circuit consisting of a NPN and a PNP BJT.

This oscillator can be designed to have low power consumption while having reasonable frequency stability with changing supply voltage and temperature. It is nevertheless quite tricky to dimension R2/R3 to provide the right voltage levels and hold-up current. Moreover the output is high impedance and the low level is not ground.

An improved version of this oscillator can be found in the complete application schematic of Fig. 8.

Since the oscillator has low current consumption, it can be supplied from the gate output of the control IC. The first gate pulse will charge C108 and the oscillator will start operating. This means it is guaranteed that the oscillator will not start drawing supply current before the controller has started operation properly. The output of the oscillator supplies positive pulses with the low level close to ground. Due to the additional resistors, the pulse length is somewhat higher than in the original simple circuit and duty-cycle is around 20%, with the given dimensioning.

The frequency is determined by R113/R117 that sets the trigger level and the timing network C109/R115. With the given values, the frequency is about 70 kHz. It is recommended to change frequency by changing C109.

In the design example, a switching frequency of 70kHz and a duty cycle of 0.277 is assumed. This leads to a maximum on time (MOT) of about 4µs, leading to a 3.9kΩ MOT resistor. Since this is outside the recommended range, a 10kΩ resistor is used.

VIII. CONCLUSION

With the DCM flyback approach, a power factor of 0.98 and THD below 10% has been achieved, even with a relatively small reflected voltage. Keeping the drain voltage low allowed the use of a 600V MOSFET that is more readily available than higher voltage alternatives. Since a SuperFET™ MOSFET can be used, the efficiency is superior to the BCM application while the cost is lower.

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