Freescale Semiconductor
Data Sheet: Advance Information

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MKW2xDxxx

MKW2xDxxx Data Sheet

Supports MKW24D512V, MKW22D512V, MKW21D512V, and MKW21D256V Products

Features

- The MKW2x is a low power, compact integrated device consisting of a high-performance 2.4 GHz IEEE 802.15.4 compliant radio transceiver and a powerful ARM Cortex-M4 MCU system with connectivity and precision mixed signal analog peripherals.
- Part of the large Kinetis MCU portfolio, the MKW2x family of devices are used to easily enable connectivity based on the ZigBee Pro network stack and application profiles for Smart Energy 1.x, Home Automation, Healthcare, and RF4CE, as well as the ZigBee IP network stack and the Smart Energy 2.0 application profile. Typical applications include Home Area Networks consisting of meters, gateways, in-home displays, and connected appliances, and also networked Building Control and Home Automation applications with lighting control, HVAC, and security.
- The MCU system of MKW2x includes a 50 MHz Cortex-M4 CPU with DSP capabilities, up to 512 KB of Flash memory, 64 KB of SRAM, and 64 KB of Flex Memory (available only on the MKW21D256V), plus a wide array of peripherals including USB, Cryptographic Acceleration, 16-bit ADC, and flexible timers.
- The radio transceiver of the MKW2x has excellent performance, with up to -102 dBm receiver sensitivity, +8 dBm maximum transmit output power, and up to 58 dBm channel rejection. Current consumption is minimized with peak transmit current of 17 mA at 0 dBm output power, and peak receive current of 15 mA in Low Power Preamble Search mode.
- The MKW2x is packaged in an 8 x 8 mm LGA with 63 total contacts, and operates between 1.8 V and 3.6 V in an ambient temperature range from -40°C to 105°C.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table of Contents

1 Ordering information

Table 1. Orderable parts details

Device	Operating Temp Range (T_A)	Package	Memory Options	Description
MKW21D256VHA5(R)	-40 to 105°C	LGA (R: tape and reel)	32 KB SRAM, 256 KB flash	Additional FlexMemory with up to 64 KB FlexNVM and up to 4 KB FlexRAM. No USB.
MKW21D512VHA5(R)	-40 to 105°C	LGA (R: tape and reel)	64 KB SRAM, 512 KB flash	Supports higher memory option and additional GPIO. No USB. No FlexNVM or FlexRAM.
MKW22D512VHA5(R)	-40 to 105°C	LGA (R: tape and reel)	64 KB SRAM, 512 KB flash	Supports full speed USB 2.0. No FlexNVM or FlexRAM.
MKW24D512VHA5(R)	-40 to 105°C	LGA (R: tape and reel)	64 KB SRAM, 512 KB flash	Supports Smart Energy 2.0 and full-speed USB 2.0. No FlexNVM or FlexRAM.

2 Features

This section provides a simplified block diagram and highlights MKW2x features.

2.1 Block diagram

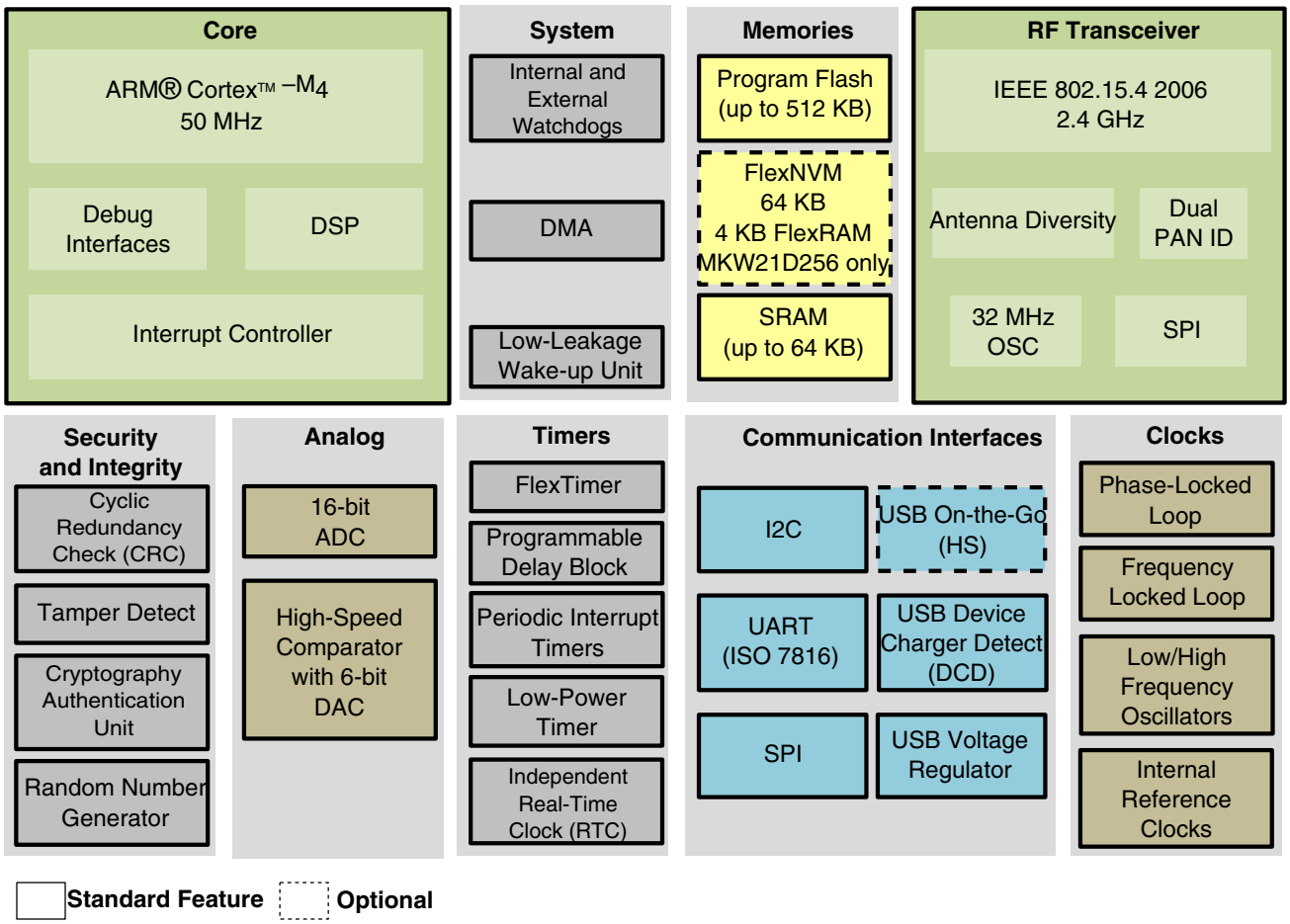


Figure 1. MKW2xDxxxV simplified block diagram

2.2 Radio features

- Fully compliant 802.15.4 Standard transceiver supports 250 kbps data rate with O-QPSK modulation in 5.0 MHz channels with direct sequence spread-spectrum (DSSS) encode and decode
- Operates on one of 16 selectable channels in the 2.4 GHz frequency ISM band
- Programmable output power
- Supports 2.36 to 2.4 GHz Medical Band (MBAN) frequencies with same modulation as IEEE 802.15.4
- Hardware acceleration for IEEE® 802.15.4 2006 packet processing

    - Random number generator
    - Support for dual PAN mode
- 32 MHz crystal reference oscillator with on board trim capability to supplement external load capacitors
- Programmable frequency clock output (CLK_OUT)
- Control port for Antenna Diversity mode
- Clocks
    - 32 MHz crystal oscillator
    - Internal 1 kHz low power oscillator
    - DC to 32 MHz external square wave input clock
- Small RF footprint
    - Differential input/output port used with external balun
    - Integrated transmit/receive switch
    - Supports single ended and diversity antenna options
    - Low external component count
    - Supports external PA and LNA

2.3 Microcontroller features

- Core:
    - ARM Cortex-M4 Core at 50 MHz (1.25 MIPS/MHz
    - Supports DSP instructions
        - Nested vectored interrupt controller (NVIC)
        - Asynchronous wake-up interrupt controller (AWIC)
        - Debug and trace capability
        - 2-pin serial wire debug (SWD)
        - IEEE 1149.1 Joint Test Action Group (JTAG)
        - IEEE 1149.7 compact JTAG (cJTAG)

        - Trace port interface unit (TPIU)
        - Flash patch and breakpoint (FPB)
        - Data watchpoint and trace (DWT)
        - Instrumentation trace macrocell (ITM)
        - Enhanced trace macrocell (ETM)
- System and power management:
    - Software and hardware watchdog with external monitor pin
    - DMA controller with 16 channels
    - Low-leakage wake-up unit (LLWU)
    - Power management controller with 10 different power modes
    - Non-maskable interrupt (NMI)
    - 128-bit unique identification (ID) number per chip
- Memories and memory interfaces:
    - Up to 512 KB Program Flash
    - Up to 64 KB of SRAM
    - In MKW21D256, FlexMemory with up to 64 KB FlexNVM and up to 4 KB FlexRAM can be partitioned.
    - EEPROM has endurance of 10 million cycles over full voltage and temperature range and read-while-write capability
    - Flash security and protection features
    - Serial flash programming interface (EzPort)
- Clocks
    - Multi-purpose clock generator
        - PLL and FLL operation
        - Internal reference clocks (32 kHz or 2 MHz)
    - Three separate crystal oscillators
        - 3 MHz to 32 MHz crystal oscillator for MCU

        - 32 kHz to 40 kHz crystal oscillator for MCU or RTC
        - 32 MHz crystal oscillator for Radio
    - Internal 1 kHz low power oscillator
    - DC to 50 MHz external square wave input clock
- Security and integrity
    - Hardware CRC module to support fast cyclic redundancy checks
    - Tamper detect and secure storage
    - Hardware random-number generator
    - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
    - 128-bit unique identification (ID) number per chip
- Analog
    - 16-bit SAR ADC
    - High-speed Analog comparator (CMP) with 6-bit DAC
- Timers
    - Up to 12 channels; 7 channels support external connections; 5 channels are internal only
    - Carrier modulator timer (CMT)
    - Programmable delay block (PDB)
    - 1x4ch programmable interrupt timer (PIT)
    - Low-power timer (LPT)
    - FlexTimers that support general-purpose PWM for motor control functions
- Communications
    - One SPI
    - Two I^2C with SMBUS support
    - Three UARTs (w/ ISO7816, IrDA, and hardware flow control)
    - One USB On-The-Go Full Speed
- Human-machine interface

    - GPIO with pin interrupt support, DMA request capability, digital glitch filter, and other pin control options
- Operating characteristics
    - Voltage range 1.8 V - 3.6 V
    - Flash memory programming down to 1.8 V
    - Temperature range (TA) -40 to 105°C

3 Transceiver description

3.1 Key specifications

MKW2x meets or exceeds all IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specifications for MKW2x are:

- ISM band:
    - RF operating frequency: 2405 MHz to 2480 MHz (center frequency range)
    - 5 MHz channel spacing
- MBAN band:
    - RF operating frequency: 2360 MHz to 2400 MHz (center frequency range)
    - MBAN channel page 9 is (2360 MHz-2390 MHz band)
        - Fc = 2363.0 + 1.0 * k in MHz for k = 0, 1, 2, ...26
    - MBAN channel page 10 is (2390 MHz-2400 MHz band)
        - Fc = 2390.0 + 1.0 * k in MHz for k = 0, 1, 2, ...8
- IEEE 802.15.4 Standard 2.4 GHz modulation scheme
    - Chip rate: 2000 kbps
    - Data rate: 250 kbps
    - Symbol rate: 62.5 kbps
    - Modulation: OQPSK

- Receiver sensitivity: -102 dBm, typical (@1% PER for 20 byte payload packet)
- Differential bidirectional RF input/output port with integrated transmit/receive switch
- Programmable output power from -35 dBm to +8 dBm.

3.2 RF interface and usage

The MKW2x RF output ports are bidirectional (diplexed between receive/transmit modes) and differential enabling interfaces with numerous off-chip devices such as a balun. When using a balun, this device provides an interface to directly connect between a single-ended antenna and the MKW2x RF ports. In addition, MKW2x provides four output driver ports that can have both drive strength and slew rate configured to control external peripheral devices. These signals designated as ANT_A, ANT_B, RX_SWITCH, and TX_SWITCH when enabled are switched via an internal hardware state machine. These ports provide control features for peripheral devices such as:

- Antenna diversity modules
- External PAs
- External LNAs
- T/R switches

3.2.1 Clock output feature

The CLK_OUT digital output can be enabled to drive the system clock to the MCU. This provides a highly accurate clock source based on the transceiver reference oscillator. The clock is programmable over a wide range of frequencies divided down from the reference 32 MHz (see Table 3). The CLK_OUT pin will be enabled upon POR. The frequency CLK_OUT default to 4 MHz (32 MHz/8).

3.3 Transceiver functions

3.3.1 Receive

The receiver has the functionality to operate in either normal run state or low power run state that can be considered as a partial power down mode. Low power run state can save a considerable amount of current by duty-cycling some sections of the receiver lineup during preamble search and is referred to as Low Power Preamble Search mode (LPPS).

The radio receiver path is based upon a near zero IF (NZIF) architecture incorporating front end amplification, one mixed signal down conversion to IF that is programmably filtered, demodulated and digitally processed. The RF front end (FE) input port is differential that shares the same off chip matching network with the transmit path.

3.3.2 Transmit

MKW2x transmits OQPSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RFOUTP, RFOUTN) are converted as single ended (SE) signals with off chip components as required.

3.3.3 Clear channel assessment (CCA), energy detection (ED), and link quality indicator (LQI)

The MKW2x supports three clear channel assessment (CCA) modes of operation including energy detection (ED) and link quality indicator (LQI). Functionality for each of these modes is as follows.

3.3.3.1 CCA mode 1

CCA mode 1 has two functions:

- To estimate the energy in the received baseband signal. This energy is estimated based on receiver signal strength indicator (RSSI).
- To determine whether the energy is greater than a set threshold.

The estimate of the energy can also be used as the Link Quality metric. In CCA Mode 1, the MKW2x must warm up from Idle to Receive mode where RSSI averaging takes place.

3.3.3.2 CCA mode 2

CCA mode 2 detects whether there is any 802.15.4 signal transmitting in the frequency band that an 802.15.4 transmitter intends to transmit. From the definition of CCA mode 2 in the 802.15.4 standard, the requirement is to detect an 802.15.4 complied signal. Whether the detected energy is strong or not is not important for CCA mode 2.

3.3.3.3 CCA mode 3

CCA mode 3 as defined by 802.15.4 standard is implemented using a logical combination of CCA mode 1 and CCA mode 2. Specifically, CCA mode 3 operates in one of two operating modes:

- CCA mode 3 is asserted if both CCA mode 1 and CCA mode 2 are asserted.
- CCA mode 3 is asserted if either CCA mode 1 or CCA mode 2 is asserted.

This mode setting is available through a programmable register.

3.3.3.4 Energy detection (ED)

Energy detection (ED) is based on receiver signal strength indicator (RSSI) and correlator output for the 802.15.4 standard. ED is an average value of signal strength. The magnitude from this measurement is calculated from the digital RSSI value that is averaged over a 128 μs duration.

3.3.3.5 Link quality indicator (LQI)

Link quality indicator (LQI) is based on receiver signal strength indicator (RSSI) or correlator output for the 802.15.4 standard. In this mode, the RSSI measurement is done during normal packet reception. LQI computations for the MKW2x are based on either digital RSSI or correlator peak values. This setting is executed through a register bit where the final LQI value is available 64 μs after preamble is detected. If a continuous update of LQI based on RSSI throughout the packet is desired, it can be read in a separate 8-bit register by enabling continuous update in a register bit.

3.3.4 Packet processor

The MKW2x packet processor performs sophisticated hardware filtering of the incoming received packet to determine if the packet is both PHY- and MAC-compliant, is addressed to this device, if the device is a PAN coordinator and whether a message is pending for the sending device. The packet processor greatly reduces the packet filtering burden on software allowing it to tend to higher-layer tasks with a lower latency and smaller software footprint.

3.3.4.1 Features

- Aggressive packet filtering to enable long, uninterrupted MCU sleep periods
- Fully compliant with both 2003 and 2006 versions of the 802.15.4 wireless standard
- Supports all frame types, including reserved types
- Supports all valid 802.15.4 frame lengths
- Enables auto-Tx acknowledge frames (no MCU intervention) by parsing of frame control field and sequence number
- Supports all source and destination address modes, and also PAN ID compression
- Supports broadcast address for PAN ID and short address mode
- Supports “promiscuous” mode, to receive all packets regardless of address- and rules-checking
- Allows frame type-specific filtering (e.g., reject all but beacon frames)
- Supports SLOTTED and non-SLOTTED modes
- Includes special filtering rules for PAN coordinator devices
- Enables minimum-turnaround Tx-acknowledge frames for data-polling requests by automatically determining message-pending status
- Assists MCU in locating pending messages in its indirect queue for data-polling end devices
- Makes available to MCU detailed status of frames that fail address- or rules-checking.
- Supports Dual PAN mode, allowing the device to exist on 2 PAN's simultaneously

- Supports 2 IEEE addresses for the device
- Supports active promiscuous mode

3.3.5 Packet buffering

The packet buffer is a 128-byte random access memory (RAM) dedicated to the storage of 802.15.4 packet contents for both TX and RX sequences. For TX sequences, software stores the contents of the packet buffer starting with the frame length byte at packet buffer address 0 followed by the packet contents at the subsequent packet buffer addresses. For RX sequences the incoming packet's frame length is stored in a register external to the packet buffer. Software will read this register to determine the number of bytes of packet buffer to read. This facilitates DMA transfer through the SPI. For receive packets, an LQI byte is stored at the byte immediately following the last byte of the packet (frame length +1). Usage of the packet buffer for RX and TX sequences is on a time-shared basis; receive packet data will overwrite the contents of the packet buffer. Software can inhibit receive-packet overwriting of the packet buffer contents by setting the PB_PROTECT bit. This will block RX packet overwriting, but will not inhibit TX content loading of the packet buffer via the SPI.

3.3.5.1 Features

- 128 byte buffer stores maximum length 802.15.4 packets
- Same buffer serves both TX and RX sequences
- The entire Packet Buffer can be uploaded or downloaded in a single SPI burst.
- Automatic address auto-incrementing for burst accesses
- Single-byte access mode supported.
- Entire packet buffer can be accessed in hibernate mode
- Under-run error interrupt supported

3.4 Dual PAN ID

In the past, radio transceivers designed for 802.15.4 and ZigBee applications allowed a device to associate to one and only one PAN (Personal Area Network) at any given time. The MKW2x represents a high-performance SiP that includes hardware support for a device to reside in two networks simultaneously. In optional Dual PAN mode, the device alternates between the two (2) PANs under hardware or software control. Hardware

support for Dual PAN operation consists of two (2) sets of PAN and IEEE addresses for the device, two (2) different channels (one for each PAN) and a programmable timer to automatically switch PANs (including on-the-fly channel changing) without software intervention. There are control bits to configure and enable Dual PAN mode, and read only bits to monitor status in Dual PAN mode. A device can be configured to be a PAN coordinator on either network, both networks or neither.

For the purpose of defining PAN in the context of Dual PAN mode, two (2) sets of network parameters are maintained; PAN0 and PAN1. PAN0 and PAN1 will be used to refer to the two (2) PANs where each parameter set uniquely identifies a PAN for Dual PAN mode. These parameters are described in Table 2.

Table 2. PAN0 and PAN1 descriptions

PAN0	PAN1
Channel0 (PHY_INT0, PHY_FRAC0)	Channel1 (PHY_INT1, PHY_FRAC1)
MacPANID0 (16-bit register)	MacPANID1 (16-bit register)
MacShortAddrs0 (16-bit register)	MacShortAddrs1 (16-bit register)
MacLongAddrs0 (64-bit registers)	MacLongAddrs1 (64-bit registers)
PANCORDNTR0 (1-bit register)	PANCORDNTR1 (1-bit register)

During device initialization if Dual PAN mode is used, software will program both parameter sets to configure the hardware for operation on two (2) networks.

4 System and power management

The MKW2x is a low power device that also supports extensive system control and power management modes to maximize battery life and provide system protection.

4.1 Modes of operation

The transceiver modes of operation include:

- Idle mode
- Doze mode
- Low power (LP) / hibernate mode
- Reset / powerdown mode
- Run mode

4.2 Power management

The MKW2x power management is controlled through programming the modes of operation. Different modes allow for different levels of power-down and RUN operation. For the receiver, programmable power modes available are:

- Preamble search
- Preamble search sniff
- Low Power Preamble Search (LPPS)
- Fast Antenna Diversity (FAD) Preamble search
- Packet decoding

5 Radio Peripherals

The MKW2x provides a set of I/O pins useful for suppling a system clock to the MCU, controlling external RF modules/circuitry, and GPIO.

5.1 Clock output (CLK_OUT)

MKW2x integrates a programmable clock to source numerous frequencies for connection with various MCUs. Package pin 39 can be used to provide this clock source as required allowing the user to make adjustments per their application requirement.

The transceiver CLK_OUT pin is internally connected to the MCU EXTAL pin so that no external connection is needed to drive the MCU clock.

Care must be taken that the clock output signal does not interfere with the reference oscillator or the radio. Additional functionality this feature supports is:

- XTAL domain can be completely gated off (hibernate mode)
- SPI communication allowed in hibernate

Table 3. CLK_OUT table

CLK_OUT_DIV [2:0]	CLK_OUT frequency
0	32 MHz[1]

Table continues on the next page...

Table 3. CLK_OUT table (continued)

CLK_OUT_DIV [2:0]	CLK_OUT frequency
1	16 MHz[1]
2	8 MHz[1]
3	4 MHz
4	2 MHz
5	1 MHz
6	62.5 kHz
7	32.786 kHz

1. May require high drive strength for proper signal integrity.

There is an enable/disable bit for CLK_OUT. When disabling, the clock output will optionally continue to run for 128 clock cycles after disablement. There is also be one (1) bit available to adjust the CLK_OUT I/O pad drive strength.

5.2 General-purpose input output (GPIO)

In addition to the MCU supported GPIOs, the radio supports 2 GPIO pins. All I/O pins will have the same supply voltage and depending on the supply, can vary from 1.8 V up to 3.6 V. When the pin is configured as a general-purpose output or for peripheral use, there will be specific settings required per use case. Pin configuration will be executed by software to adjust input/output direction and drive strength, capability. When the pin is configured as a general-purpose input or for peripheral use, software (see Table 4) can enable a pull-up or pull-down device. Immediately after reset, all pins are configured as high-impedance general-purpose inputs with internal pull-up devices enabled.

Features for these pins include:

- Programmable output drive strength
- Programmable output slew rate
- Hi-Z mode
- Programmable as outputs or inputs (default)

Table 4. Pin configuration summary

Pin function configuration	Details	Tolerance			Units
		Min.	Typ.	Max.	
I/O buffer full drive mode[1]	Source or sink	—	±10	—	mA
I/O buffer partial drive mode[2]	Source or sink	—	±2	—	mA

Table continues on the next page...

Table 4. Pin configuration summary (continued)

Pin function configuration	Details	Tolerance			Units
		Min.	Typ.	Max.	
I/O buffer high impedance[3]	Off state	—	—	10	nA
No slew, full drive	Rise and fall time[4]	2	4	6	ns
No slew, partial drive	Rise and fall time	2	4	6	ns
Slew, full drive	Rise and fall time	6	12	24	ns
Slew, partial drive	Rise and fall time	6	12	24	ns
Propagation delay[5], no slew	Full drive[6]	—	—	11	ns
Propagation delay, no slew	Partial drive[7]	—	—	11	ns
Propagation delay, slew	Full drive	—	—	50	ns
Propagation delay, slew	Partial drive	—	—	50	ns

1. For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.
2. For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.
3. Leakage current applies for the full range of possible input voltage conditions.
4. Rise and fall time values in reference to 20% and 80%
5. Propagation Delay measured from/to 50% voltage point.
6. Full drive values provided are in reference to a 75 pF load.
7. Partial drive values provided are in reference to a 15 pF load.

5.2.1 Serial peripheral interface (SPI)

The MKW2x SiP uses a SPI interface allowing the MCU to communicate with the radio's register set and packet buffer. The SPI is a slave-only interface; the MCU must drive R_SSEL_B, R_SCLK and R_MOSI. Write and read access to both direct and indirect registers is supported, and transfer length can be single-byte or bursts of unlimited length. Write and read access to the Packet buffer can also be single-byte or a burst mode of unlimited length.

The SPI interface is asynchronous to the rest of the IC. No relationship between R_SCLK and MKW2x's internal oscillator is assumed. And no relationship between R_SCLK and the CLK_OUT pin is assumed. All synchronization of the SPI interface to the IC takes place inside the SPI module. SPI synchronization takes place in both directions; register writes and register reads. The SPI is capable of operation in all power modes, except Reset. Operation in hibernate mode allows most transceiver registers and the complete packet buffer to be accessed in the lowest-power operating state enabling minimal power consumption, especially during the register-initialization phase of the radio.

The SPI design features a compact, single-byte control word, reducing SPI access latency to a minimum. Most SPI access types require only a single-byte control word, with the address embedded in the control word. During control word transfer (the first byte of any

SPI access), the contents of the IRQSTS1 register (MKW2x radio's highest-priority status register) are always shifted out so that the MCU gets access to IRQSTS1, with the minimum possible latency, on every SPI access.

5.2.1.1 Features

- 4-wire industry standard interface, supported by all MCUs
- SPI R_SCLK maximum frequency 16 MHz (for SPI write accesses)
- SPI R_SCLK maximum frequency 9 MHz (for SPI read accesses)
- Write and read access to all radio registers (direct and indirect)
- Write and read access to packet buffer
- SPI accesses can be single-byte or burst
- Automatic address auto-incrementing for burst accesses
- The entire packet buffer can be uploaded or downloaded in a single SPI burst
- Entire packet buffer and most registers can be accessed in hibernate mode
- Built-in synchronization inside the SPI module to/from the rest of the radio

5.2.2 Antenna diversity

To improve the reliability of RF connectivity to long range applications, the antenna diversity feature is supported without using the MCU through use of four dedicated control pins (package pins 44, 45, 46, and 47).

Fast antenna diversity (FAD) mode supports this radio feature and, when enabled, will allow the choice of selection between two antennas during the preamble phase. By continually monitoring the received signal, the FAD block will select the first antenna of which the received signal has a correlation factor above a predefined progammable threshold. The FAD accomplishes the antenna selection by sequentially switching between the two antennas testing for the presence of suitably strong s0 symbol where the first antenna to reach this condition is then selected for the reception of the packet.

The antenna's are monitored for a period of 28 μs each. The antenna switching is continued until 1.5 valid s0 symbols are detected. The demodulator then continues with normal preamble search before declaring “Preamble Detect”.

6 MKW2x operating modes

For the discussion of this topic, the primary radio and MCU operating modes are combined so that overall power consumption can then be derived. Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. Both the radio and MCU's power modes are described as follows.

The radio has 6 primary operating modes:

- Reset / power down
- Low power (LP) / hibernate
- Doze (low power with reference oscillator active)
- Idle
- Receive
- Transmit

Table 5 lists and describes the transceivers power modes and consumption.

Table 5. Transceiver Power Modes

Mode	Definition	Current consumption[1]
Reset / powerdown	All IC functions off, leakage only. $\overline{RST}$ asserted.	< 100 nA
Low power / hibernate	Crystal reference oscillator off. (SPI is functional.)	< 1 µA
Doze[2]	Crystal reference oscillator on but CLK_OUT output available only if selected.	500 µA[3] (no CLK_OUT)
Idle	Crystal reference oscillator on with CLK_OUT output available only if selected.	700 µA[3] (no CLK_OUT)
Receive	Crystal reference oscillator on. Receiver on.	< 19.5 mA [4] 15 mA, LPPS mode
Transmit	Crystal reference oscillator on. Transmitter on.	< 18 mA [5]

1. Conditions: VBAT and VBAT_2 = 2.7 V, nominal process @ 25°C
2. While in Doze mode, 4 MHz max frequency can be selected for CLK_OUT.
3. Typical

4. Signal sensitivity = -102 dBm
5. RF output = 0 dBm

The MCU has a variety of operating modes. For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

7 MKW2x electrical characteristics

7.1 Radio recommended operating conditions

Table 6. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BAT} = VDD_{INT})	V_{BAT}, VDD_{INT}	1.8	2.7	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
Ambient Temperature Range	TA	-40	25	105	°C
Logic Input Voltage Low	VIL	0	—	30% VDDINT	V
Logic Input Voltage High	VIH	70% VDDINT	—	VDDINT	V
SPI Clock Rate	f_{SPI}	—	—	16.0	MHz
RF Input Power	Pmax	—	—	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	32 MHz only			

7.2 Ratings

7.2.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

7.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

7.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

7.2.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.6	V
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

8 MCU Electrical characteristics

8.1 Maximum ratings

Table 7. Maximum ratings

Requirement	Description	Symbol	Rating level	Unit
Power Supply Voltage		VBAT, VBAT2	-0.3 to 3.6	Vdc
Digital Input Voltage		Vin	-0.3 to (VDDINT + 0.3)	Vdc
RF Input Power		Pmax	+10	dBm
Note: Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.				
ESD[1]	Human Body Model	HBM	±2000	Vdc
	Machine Model	MM	±200	Vdc
	Charged Device Model	CDM	±750	Vdc
EMC[2]	Power Electro-Static Discharge / Direct Contact	PESD	No damage / latch up to ±4000	Vdc
			No soft failure / reset to ±1000	
	Power Electro-Static Discharge / Indirect Contact		No damage / latch up to ±6000	Vdc
			No soft failure / reset to ±1000	
	Langer IC / EFT / P201	EFT (Electro Magnetic Fast Transient)	No damage / latch up to ±5	Vdc
			No soft failure / reset to ±5	
	Langer IC / EFT / P201		No damage / latch up to ±300	Vdc
			No soft failure / reset to ±150	
Junction Temperature		T_J	+125	°C
Storage Temperature Range		T_{stg}	-65 to +165	°C

1. Electrostatic discharge on all device pads meet this requirement
2. Electromagnetic compatibility for this product is low stress rating level

Note

Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.

8.2 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

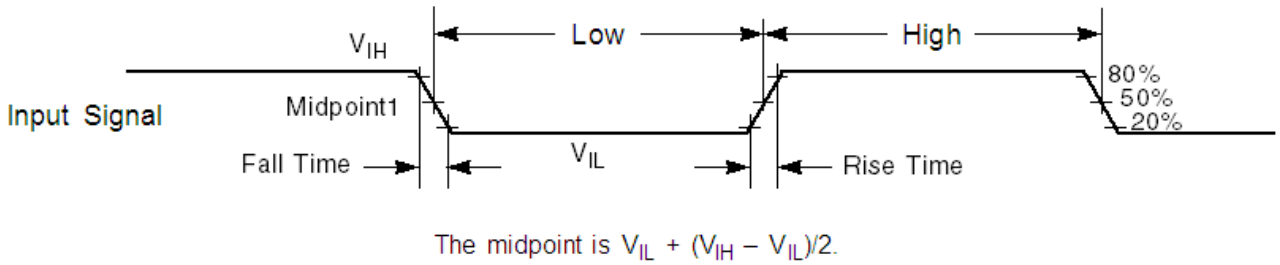


Figure 2. Input signal measurement reference

8.3 Nonswitching electrical specifications

8.3.1 Voltage and current operating requirements

Table 8. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.8	3.6	V	
V_{DDA}	Analog supply voltage	1.8	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.8	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	I/O pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -3 —	 — +3	 mA	1

Table continues on the next page...

Table 8. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	 mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

8.3.2 LVD and POR operating requirements

Table 9. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 10. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

8.3.3 Voltage and current operating behaviors

Table 11. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = - 9 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3 mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				
	• @ full temperature range	—	1.0	µA	1
	• @ 25 °C	—	0.1	µA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	µA	
R_{PU}	Internal pullup resistors	22	50	kΩ	2
R_{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

8.3.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 12. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • 1.71 V/(V_{DD} slew rate) ≤ 300 µs • 1.71 V/(V_{DD} slew rate) > 300 µs	 — —	 300 1.7 V / (V_{DD} slew rate)	µs	1
	• VLLS1 → RUN	—	150	µs	
	• VLLS2 → RUN	—	79	µs	
	• VLLS3 → RUN	—	79	µs	
	• LLS → RUN	—	6	µs	
	• VLPS → RUN	—	5.2	µs	
	• STOP → RUN	—	5.2	µs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

8.3.5 Power consumption operating behaviors

Table 13. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8 V • @ 3.0 V	 — —	 12.98 12.93	 14 13.8	 mA mA	2

Table continues on the next page...

Table 13. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8 V	—	17.04	19.3	mA	
	• @ 3.0 V					
	• @ 25°C	—	17.01	18.9	mA	
	• @ 125°C	—	19.8	21.3	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.95	9.5	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.88	7.4	mA	5
I_{DD_STOP}	Stop mode current at 3.0 V	—			μA	
	• @ –40 to 25°C		320	436		
	• @ 50°C		360	489		
	• @ 70°C		410	620		
	• @ 105°C		610	1100		
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	754	—	μA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	437	—	μA	8
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V	—			μA	
	• @ –40 to 25°C		7.33	24.2		
	• @ 50°C		14	32		
	• @ 70°C		28	48		
	• @ 105°C		110	280		
I_{DD_LLS}	Low leakage stop mode current at 3.0 V	—			μA	
	• @ –40 to 25°C		3.14	4.8		
	• @ 50°C		6.48	28.3		
	• @ 70°C		13.85	44.6		
	• @ 105°C		55.53	71.3		
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V	—			μA	
	• @ –40 to 25°C		2.19	3.4		
	• @ 50°C		4.35	4.35		
	• @ 70°C		8.92	24.6		
	• @ 105°C		35.33	45.3		
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V	—			μA	
	• @ –40 to 25°C		1.77	3.1		
	• @ 50°C		2.81	13.8		
	• @ 70°C		5.20	22.3		
	• @ 105°C		19.88	34.2		

Table continues on the next page...

Table 13. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	1.03 1.92 4.03 17.43	1.8 7.5 15.9 28.7	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.543 1.36 3.39 16.52	1.1 7.58 14.3 24.1	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.359 1.03 2.87 15.20	0.95 6.8 15.4 25.3	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.91 1.1 1.5 4.3	1.1 1.35 1.85 5.7	µA	9

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32 kHz oscillator current and RTC operation.

8.3.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

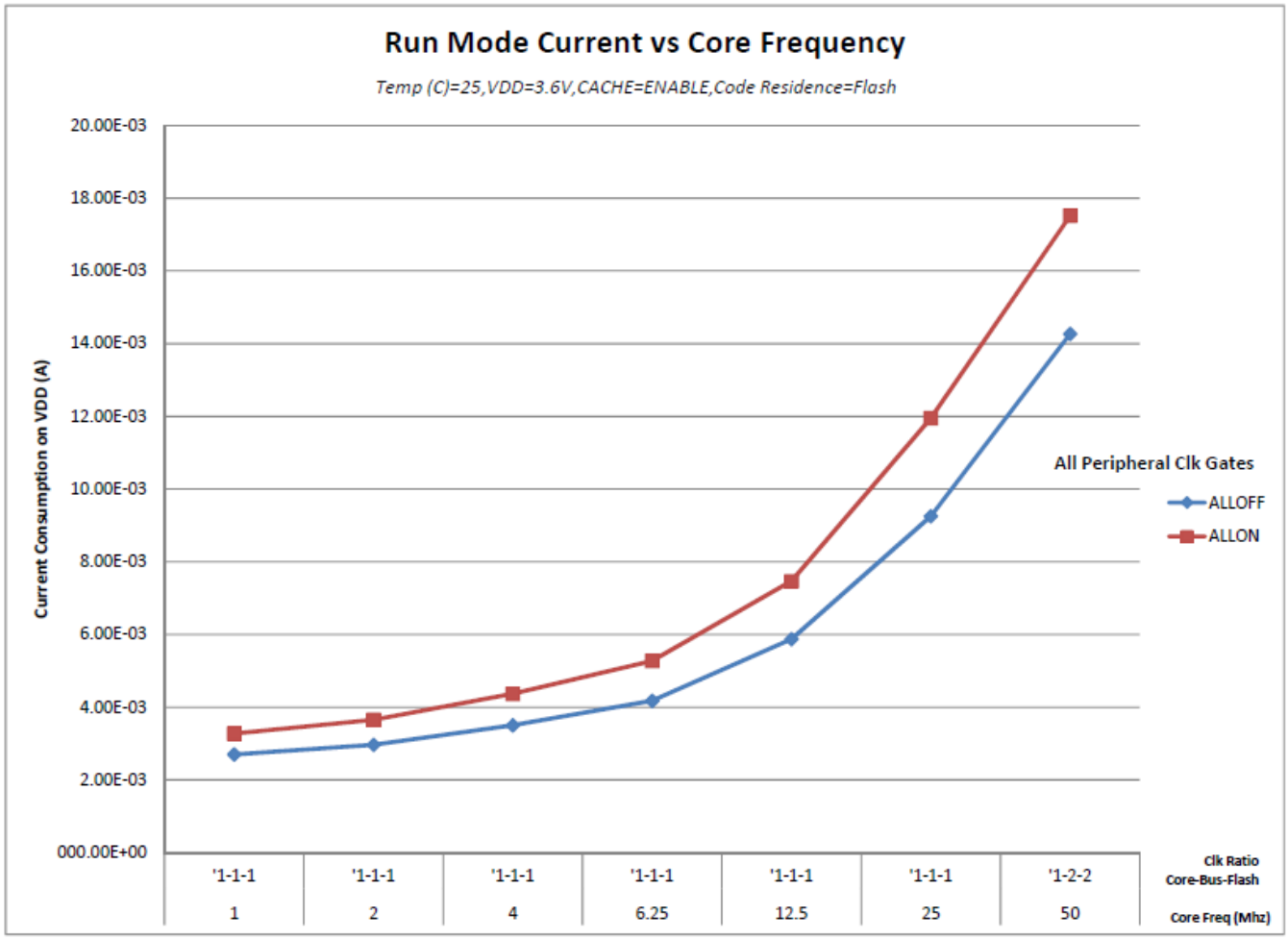


Figure 3. Run mode supply current vs. core frequency

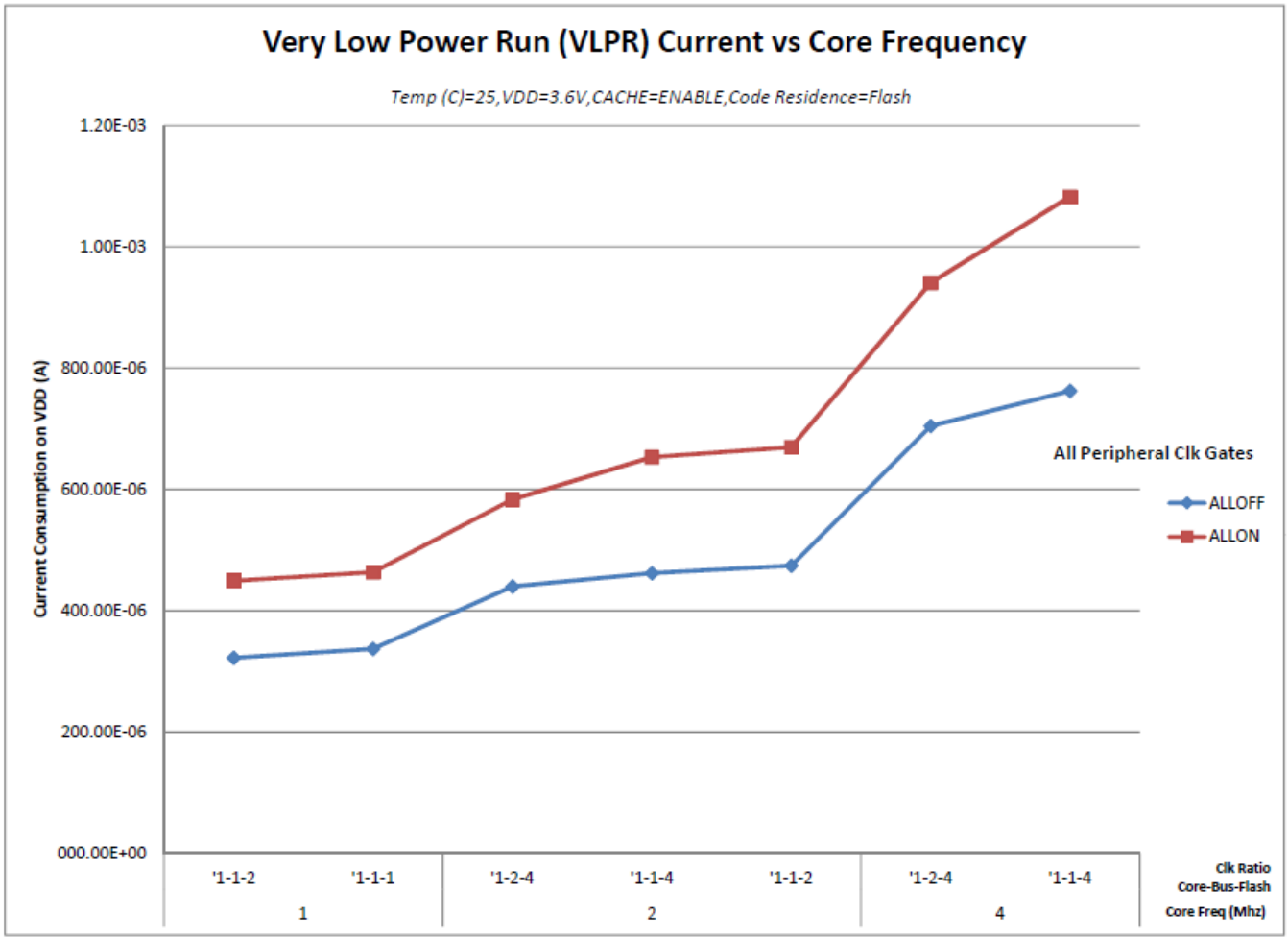


Figure 4. VLPR mode supply current vs. core frequency

8.3.6 EMC radiated emissions operating behaviors

Table 14. EMC radiated emissions operating behaviors [1]

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	19	dBµV	2, 3
V_{RE2}	Radiated emissions voltage, band 2	50–150	21	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	19	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	11	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	3, 4

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.
2. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

3. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 48 MHz, f_{BUS} = 48MHz
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

8.3.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

8.3.8 Capacitance attributes

Table 15. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

8.4 Switching specifications

8.4.1 Device clock specifications

Table 16. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	

Table continues on the next page...

Table 16. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

8.4.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

Table 17. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Port rise and fall time (high drive strength) • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 13 7 36 24	 ns ns ns ns	4
	Port rise and fall time (low drive strength) • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 12 6 36 24	 ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.

3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

8.5 Thermal specifications

8.5.1 Thermal operating requirements

Table 18. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

8.5.2 Thermal attributes

Board type	Symbol	Description	80 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	35	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	39	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	29	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	19	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8	°C/W	5

Table continues on the next page...

Board type	Symbol	Description	80 LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

8.6 Peripheral operating requirements and behaviors

8.6.1 Core modules

8.6.1.1 JTAG electricals

Table 19. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns

Table continues on the next page...

Table 19. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 20. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.8	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

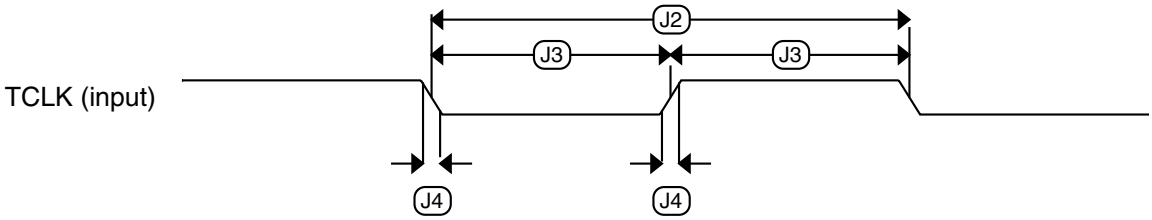


Figure 5. Test clock input timing

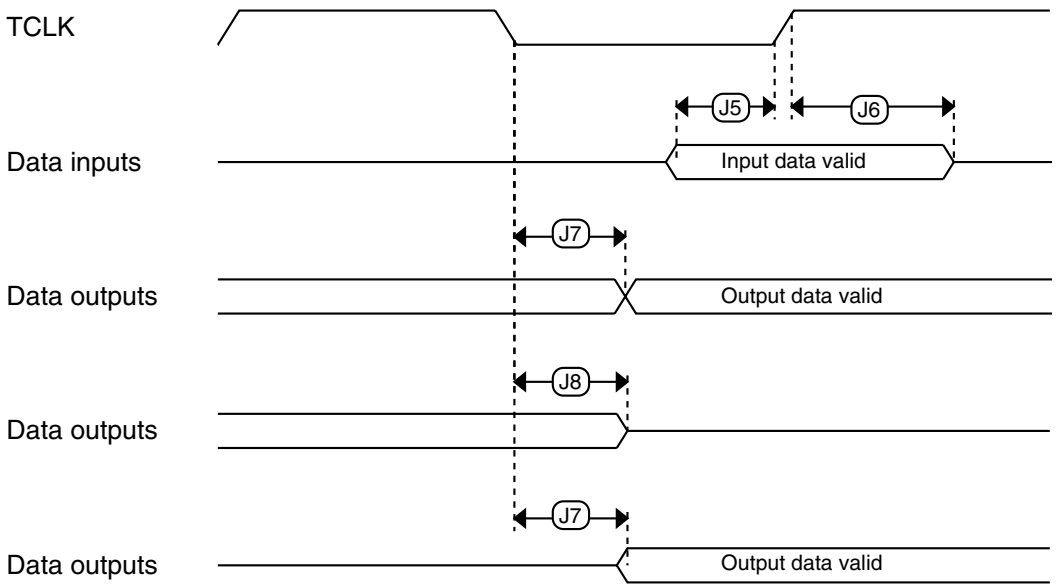


Figure 6. Boundary scan (JTAG) timing

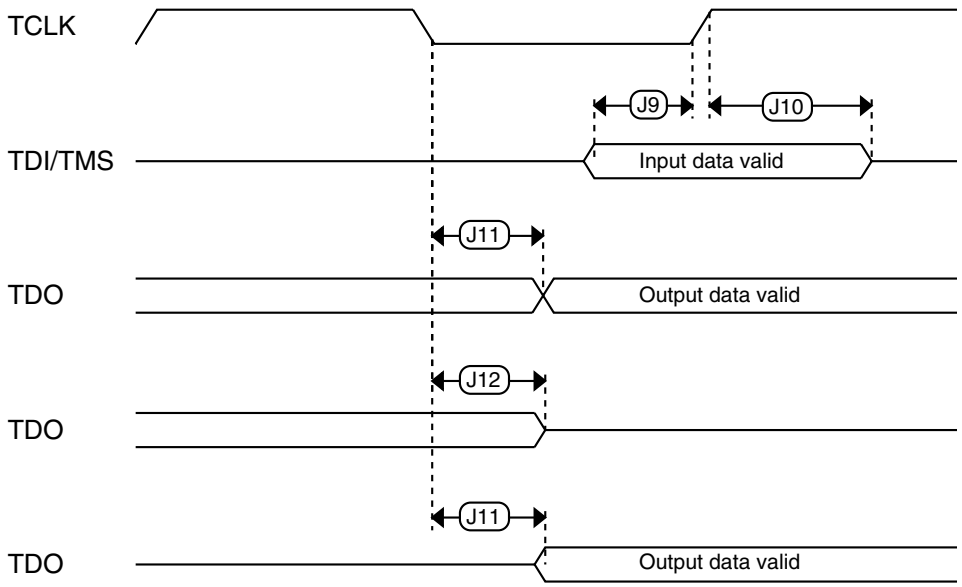


Figure 7. Test Access Port timing

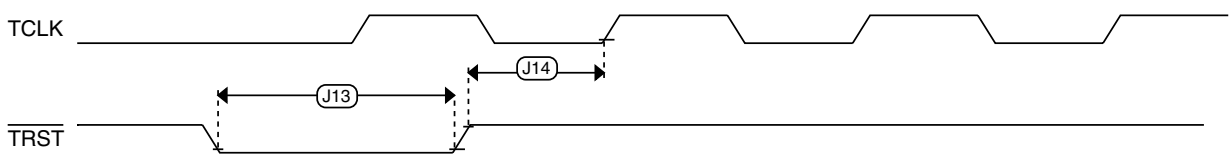


Figure 8. $\overline{\text{TRST}}$ timing

8.6.2 System modules

There are no specifications necessary for the device's system modules.

8.6.3 Clock modules

8.6.3.1 MCG specifications

Table 21. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	±1	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	

Table continues on the next page...

Table 21. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz	— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	7
PLL						
f_{vco}	VCO operating frequency	48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)	—	1200	—	µA	8
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)	—	700	—	µA	8
f_{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	 — —	 120 75	 — —	 ps ps	9
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	 — —	 1350 600	 — —	 ps ps	9
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8.6.3.2 Oscillator electrical specifications

8.6.3.2.1 Oscillator DC electrical specifications

Table 22. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.8	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	5	—	µA	
	• 4 MHz	—	500	—	µA	
	• 8 MHz (RANGE=01)	—	600	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

Table 22. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

8.6.3.2.2 Oscillator frequency specifications

Table 23. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.

3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

8.6.3.3 32 kHz oscillator electrical characteristics

8.6.3.3.1 32 kHz oscillator DC electrical specifications

Table 24. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.8	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

8.6.3.3.2 32 kHz oscillator frequency specifications

Table 25. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

8.6.4 Memories and memory interfaces

8.6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 26. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.6.4.1.2 Flash timing specifications — commands

Table 27. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk64k}$	• 64 KB data flash	—	—	0.9	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.7	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
	Erase Flash Block execution time					2
$t_{ersblk64k}$	• 64 KB data flash	—	58	580	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 bytes flash	—	2.4	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	4.7	—	ms	
$t_{pgmsec2k}$	• 2 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	250	2000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

Table continues on the next page...

Table 27. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	70	150	µs	
$t_{swapx04}$	• control code 0x04	—	70	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	
	Program Partition for EEPROM execution time					
$t_{pgmpart64k}$	• 64 KB FlexNVM	—	138	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	70	—	µs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b64k}$	• 64 KB EEPROM backup		475	2000	µs	
Word-write to FlexRAM for EEPROM operation						
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

8.6.4.1.3 Flash high voltage current behaviors

Table 28. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

8.6.4.1.4 Reliability specifications

Table 29. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
	Data Flash					
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
	FlexRAM as EEPROM					
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ °C.
3. Write endurance represents the number of writes to each FlexRAM location at -40 °C ≤Tj ≤ °C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

8.6.4.2 EzPort switching specifications

Table 30. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.8	3.6	V

Table continues on the next page...

Table 30. EzPort switching specifications (continued)

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—		ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

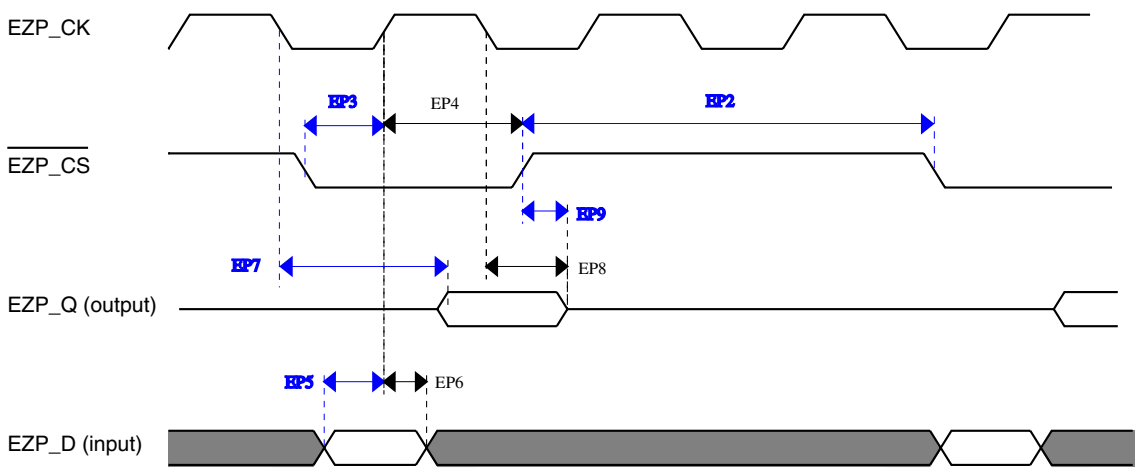


Figure 9. EzPort Timing Diagram

8.6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

8.6.5.1 Drylce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local Freescale sales representative.

8.6.6 Analog

8.6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 1 and Table 32 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

8.6.6.1.1 16-bit ADC operating conditions

Table 31. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.8	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	7

Table continues on the next page...

Table 31. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. V_{REFH} is internally tied to V_{DDA}.
4. V_{REFL} is internally tied to V_{SSA}.
5. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
6. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
7. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

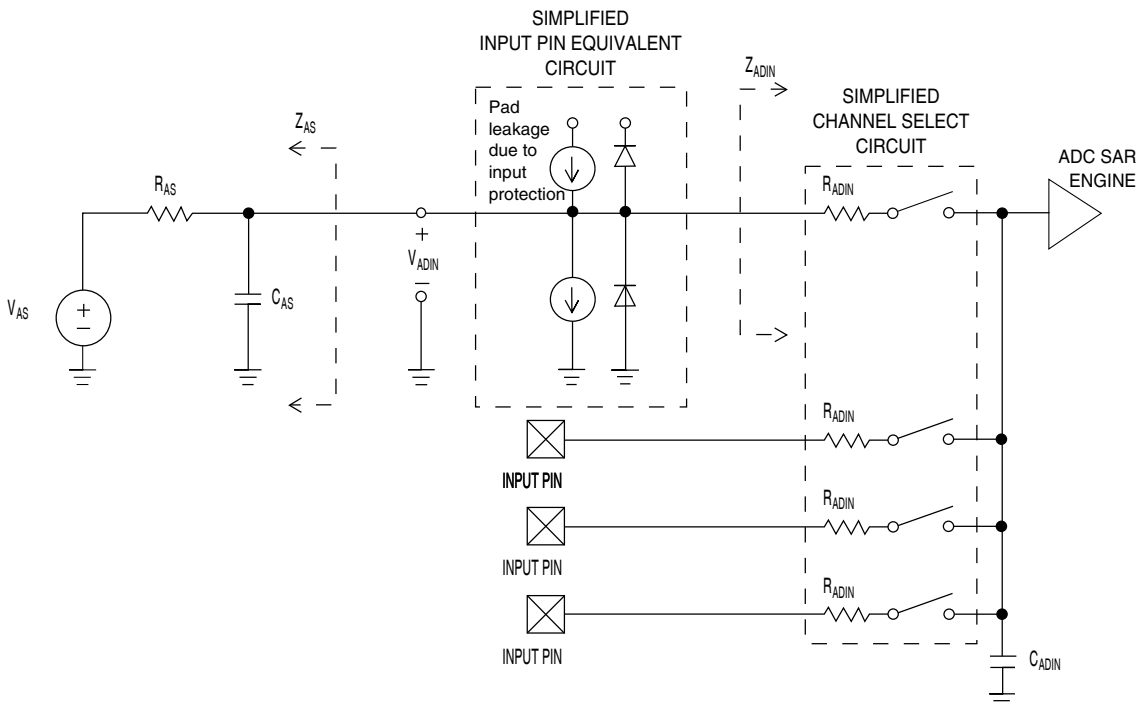


Figure 10. ADC input impedance equivalency diagram

8.6.6.1.2 16-bit ADC electrical characteristics

Table 32. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	 dB dB	7

Table continues on the next page...

Table 32. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
E_{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

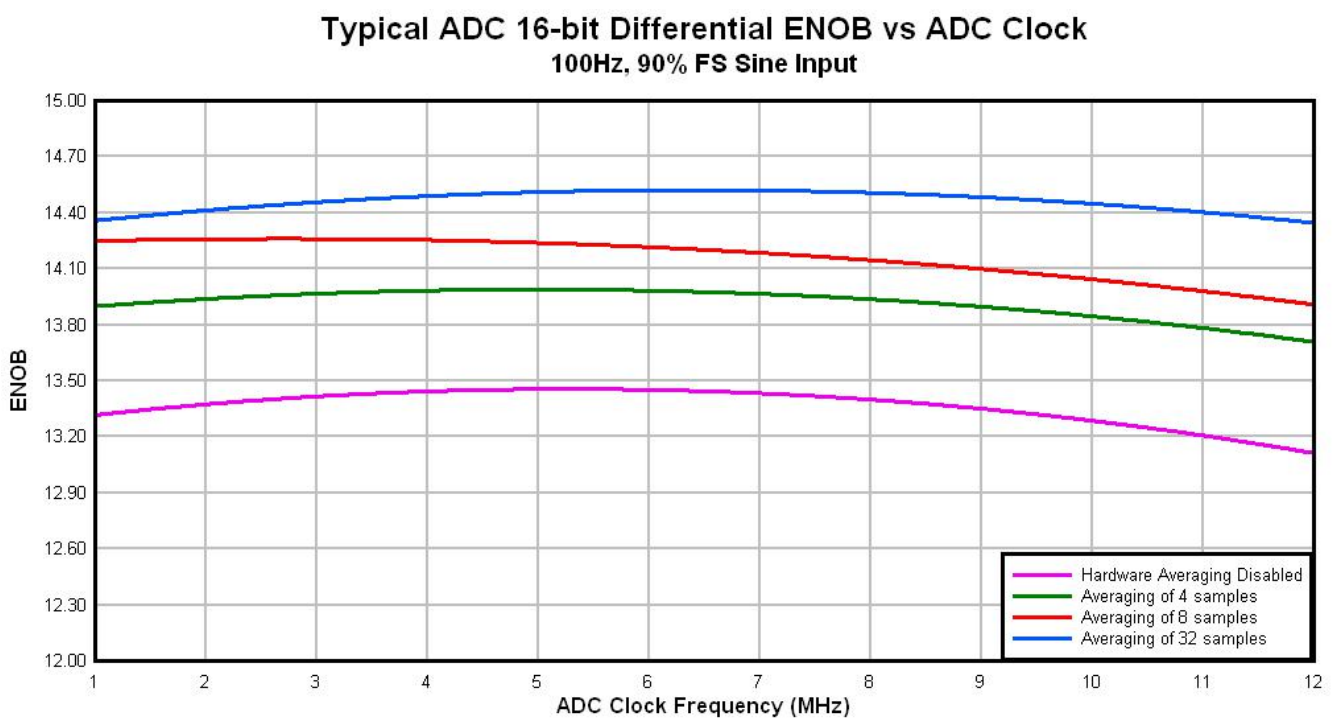


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit differential mode

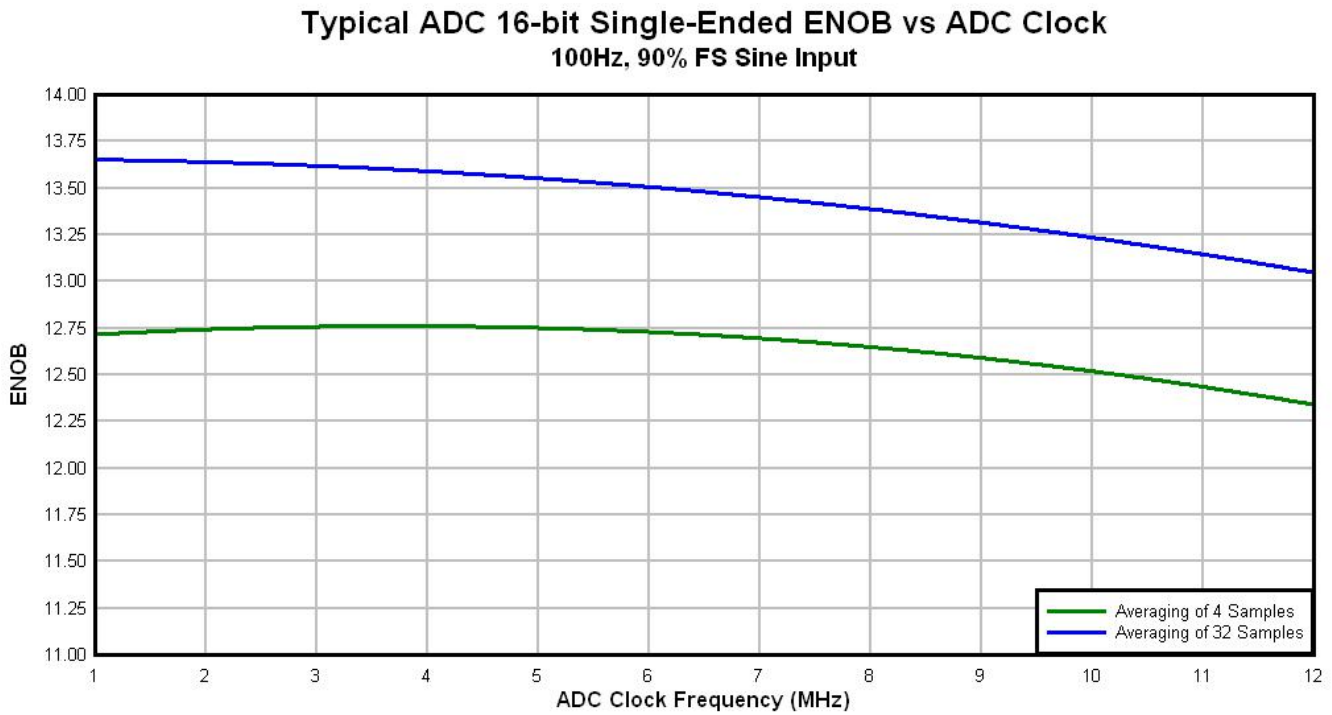


Figure 12. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

8.6.6.2 CMP and 6-bit DAC electrical specifications

Table 33. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.8	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA

Table continues on the next page...

Table 33. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

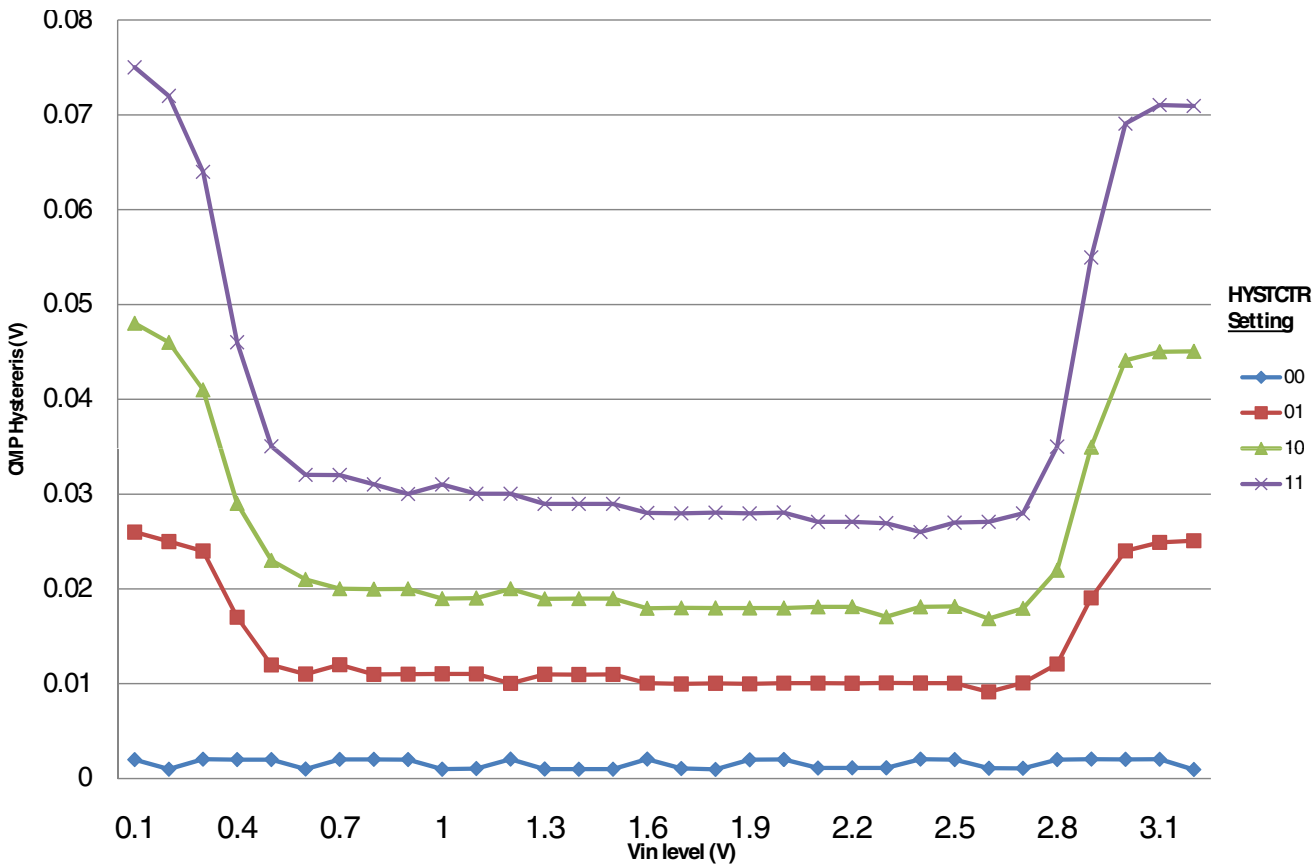


Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

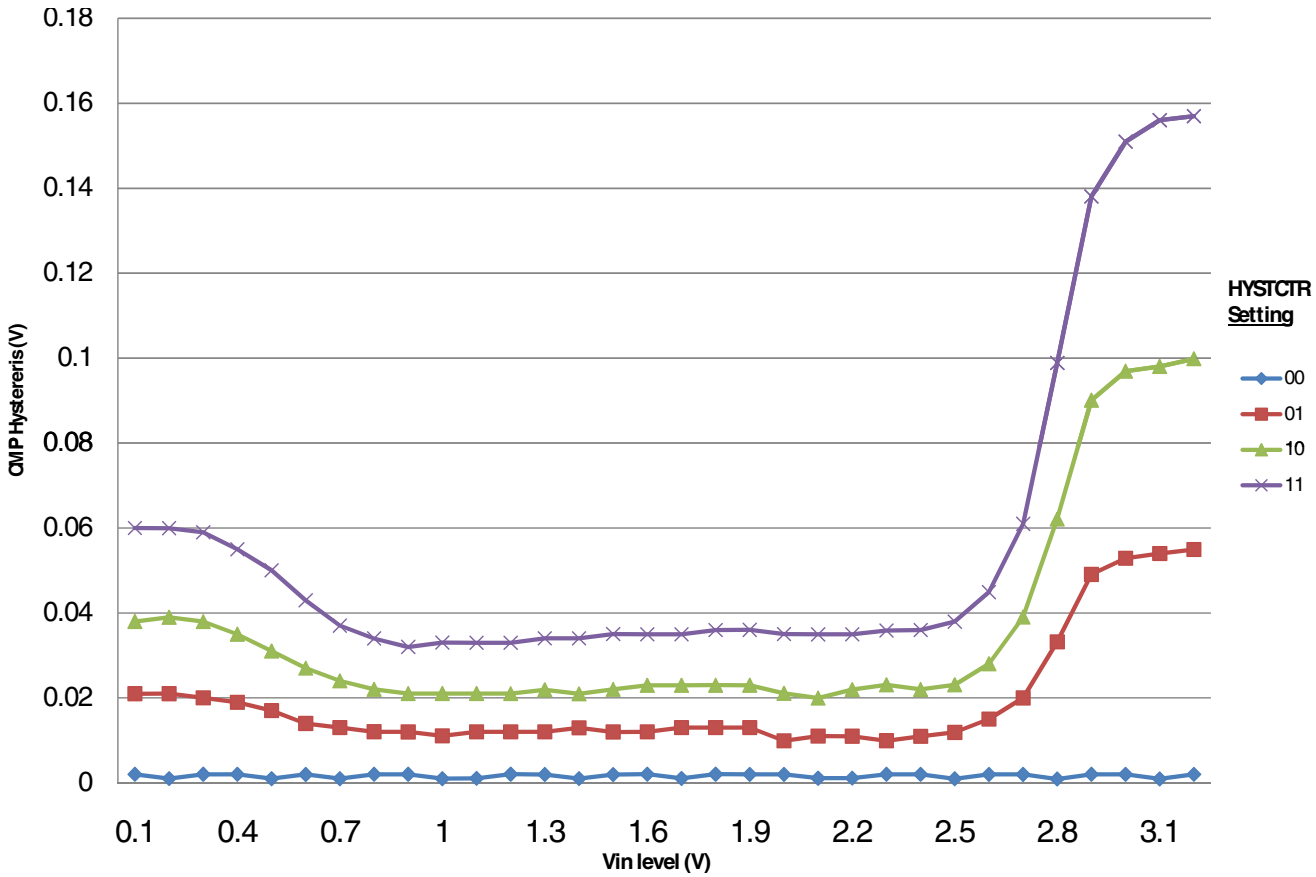


Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

8.6.7 Timers

See General Switching Specifications.

8.6.8 Communication interfaces

8.6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

8.6.8.2 USB DCD electrical specifications

Table 34. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

8.6.8.3 VREG electrical specifications

Table 35. VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.27	30	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	 — —	 650 —	 — 4	 nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

8.6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 36. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

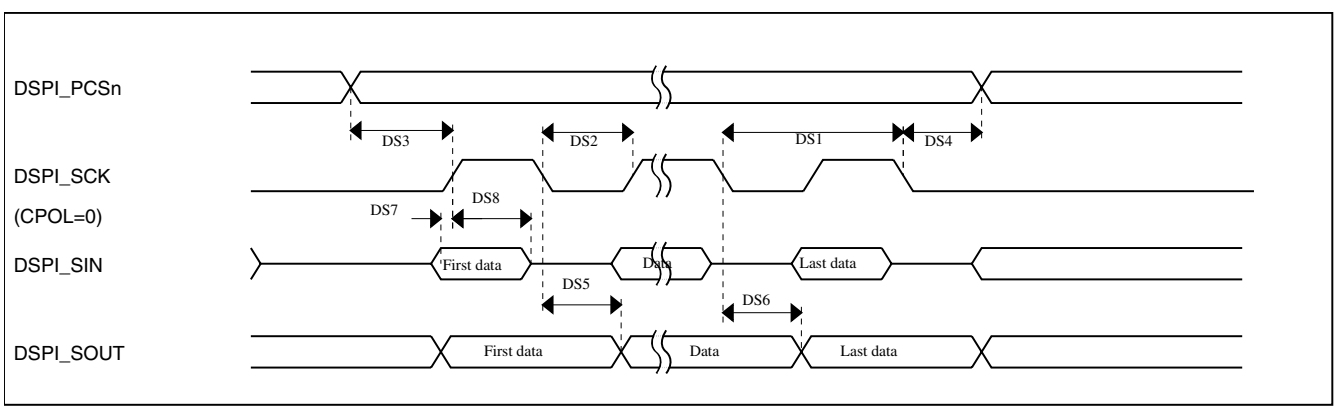


Figure 15. DSPI classic SPI timing — master mode

Table 37. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns

Table continues on the next page...

Table 37. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

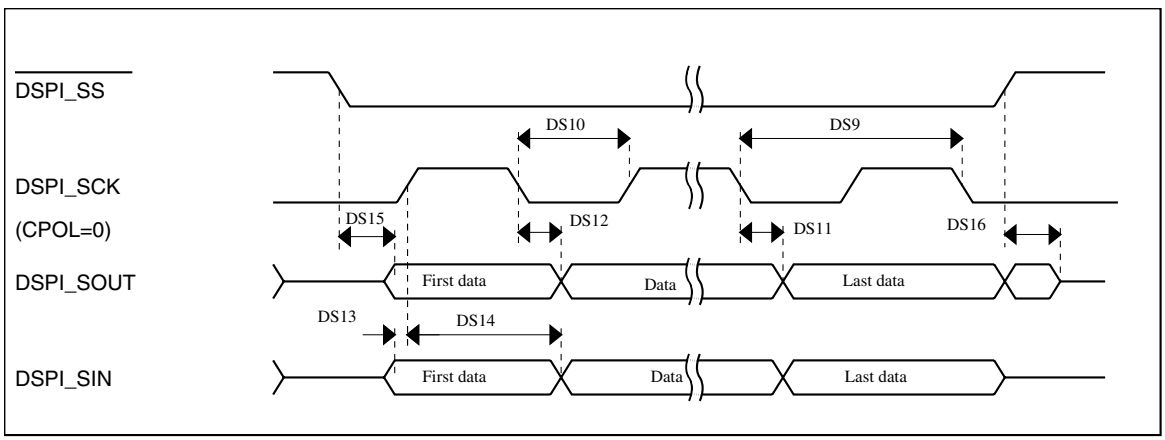


Figure 16. DSPI classic SPI timing — slave mode

8.6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.8	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3

Table continues on the next page...

Table 38. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

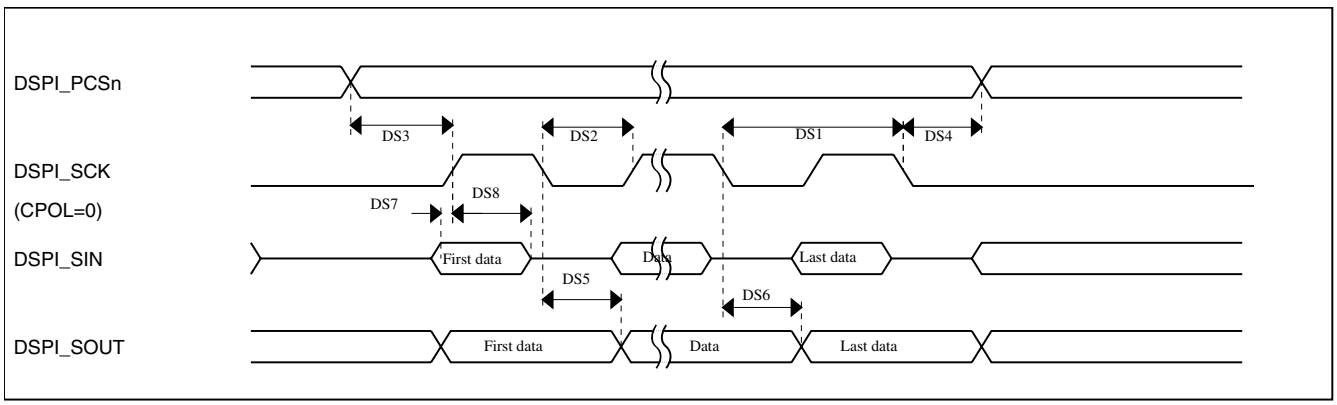


Figure 17. DSPI classic SPI timing — master mode

Table 39. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.8	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

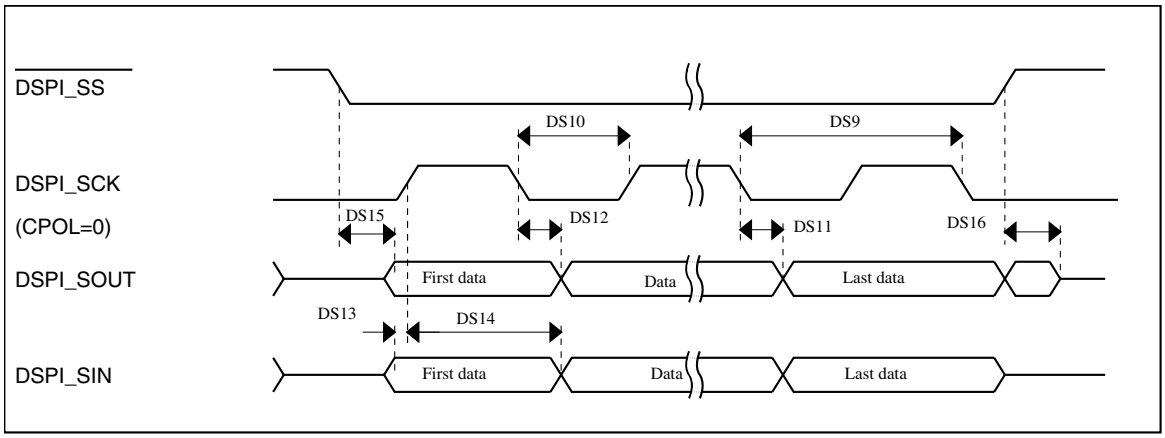


Figure 18. DSPI classic SPI timing — slave mode

8.6.8.6 I²C

See General Switching Specifications.

8.6.8.7 UART

See General Switching Specifications.

8.6.8.8 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Due to a limited set of pin availability in the SiP, the I2S/SAI block is usable only for receive mode and must be configured as a slave.

Table 40. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.8	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns

Table continues on the next page...

Table 40. I2S/SAI master mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

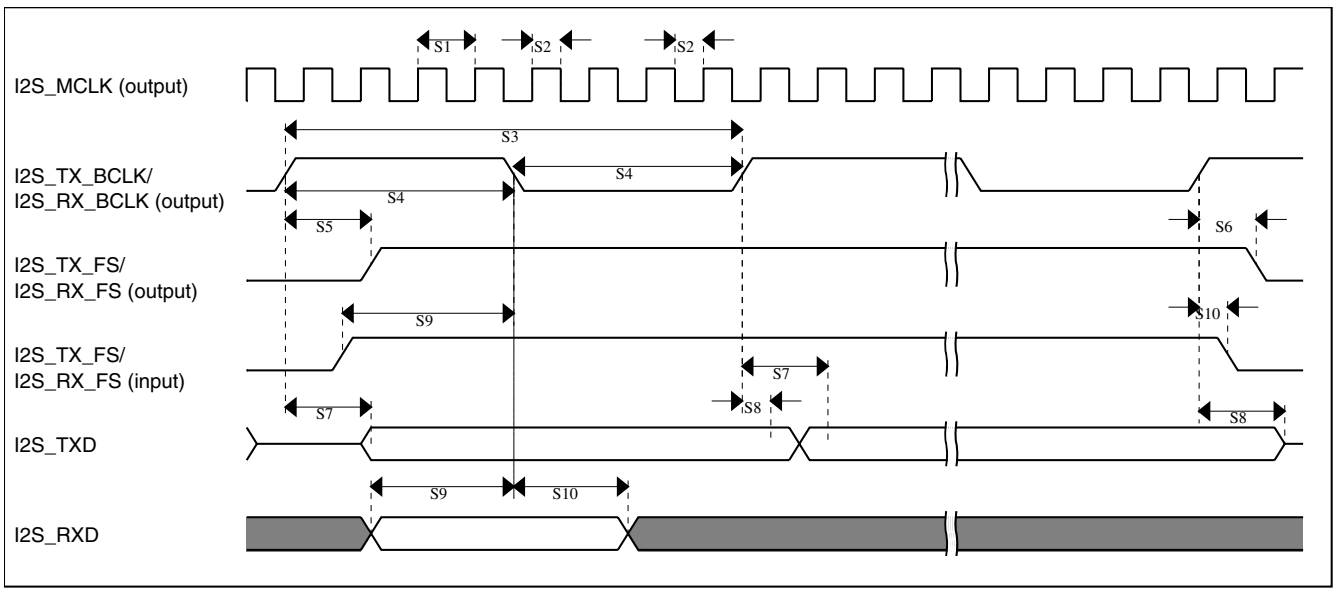


Figure 19. I2S/SAI timing — master modes

Table 41. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.8	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

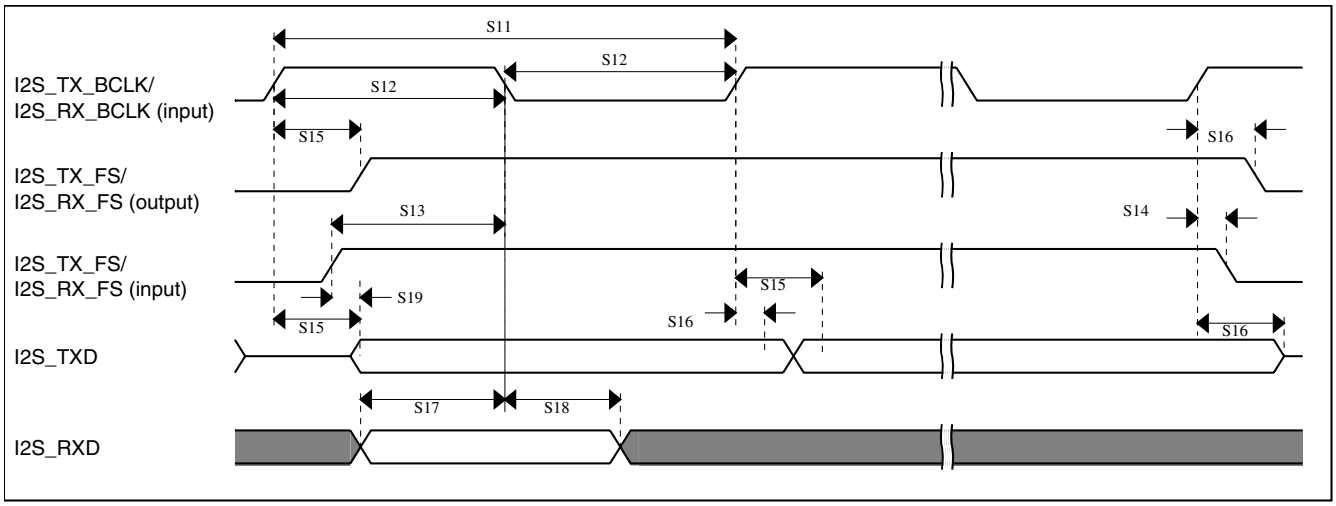


Figure 20. I2S/SAI timing — slave modes

8.6.8.9 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Due to a limited set of pin availability in the SiP, the I2S/SAI block is usable only for receive mode and must be configured as a slave.

Table 42. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.8	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

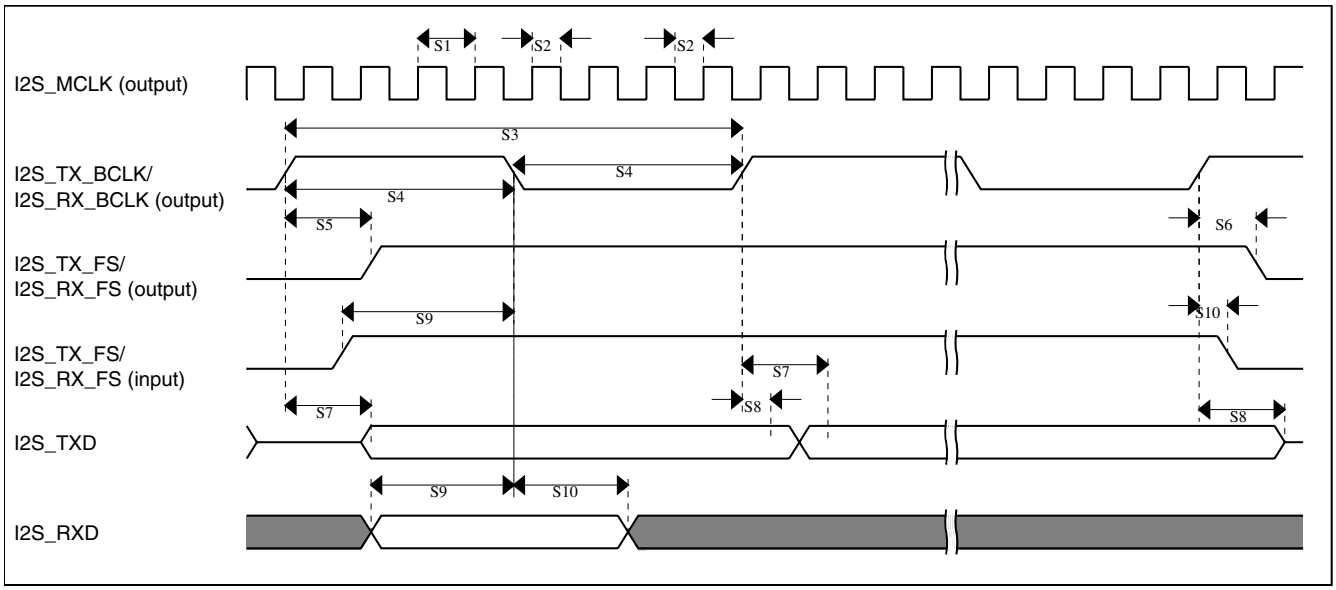


Figure 21. I2S/SAI timing — master modes

Table 43. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.8	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

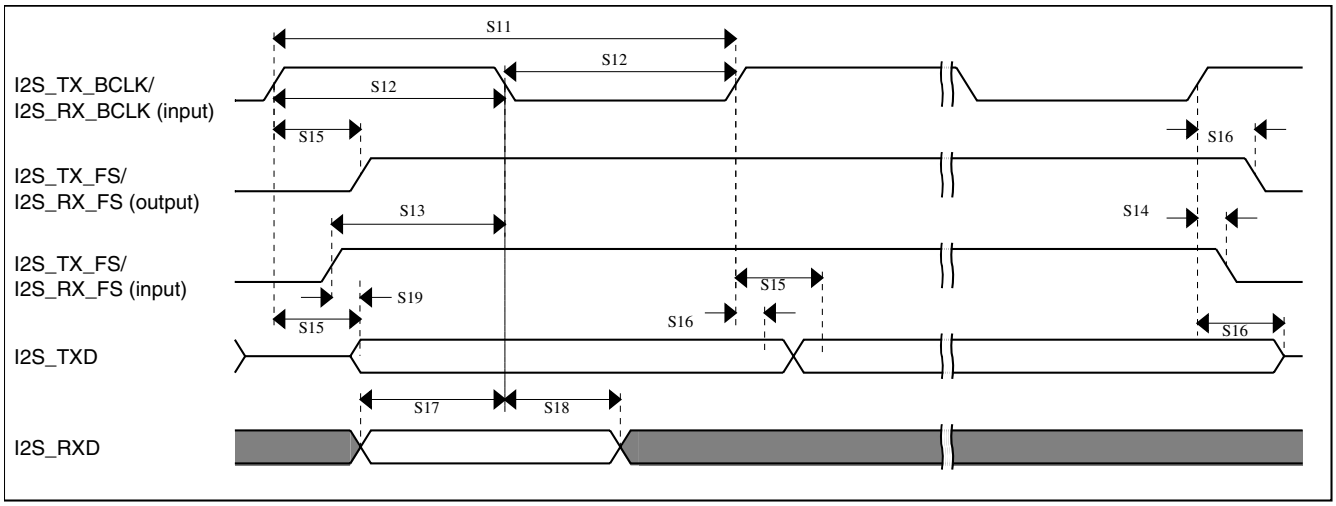


Figure 22. I2S/SAI timing — slave modes

9 Transceiver Electrical Characteristics

9.1 DC electrical characteristics

Table 44. DC electrical characteristics (V_{BAT}, V_{DDINT} = 2.7 V, T_A=25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (VBAT + VDDINT)	$I_{leakage}$	—	<60	<100	nA
Reset / power down[1]	I_{CCH}	—	<1	—	µA
Hibernate	I_{CCD}	—	500	—	µA
Doze (No CLK_OUT)	I_{CCI}	—	700	—	µA
Idle (No CLK_OUT)	I_{CCT}	—	17	18	mA
Transmit mode (0 dBm nominal output power)	I_{CCR}	—	19	19.5	mA
Receive mode			15 (LPPS)		
Input current (VIN = 0 V or VDDINT) (All digital inputs)	I_{IN}	—	—	±1	µA
Input low voltage (all digital inputs)	V_{IL}	0	—	30% V_{DDINT}	V
Input high voltage (all digital inputs)	V_{IH}	70% V_{DDINT}	—	V_{DDINT}	V
Output high voltage (IOH = -1 mA) (all digital outputs)	V_{OH}	80% V_{DDINT}	—	V_{DDINT}	V
Output low voltage (IOL = 1 mA) (all digital outputs)	V_{OL}	0	—	20% V_{DDINT}	V

1. To attain specified low power current, all GPIO and other digital IO must be handled properly.

9.2 AC electrical characteristics

Table 45. Receiver AC electrical characteristics (V_{BAT}, V_{DDINT} = 2.7 V, T_A=25 °C, f_{ref} = 32 MHz unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% packet error rate (PER) (–40 to +105 °C)	SENSper	—	–99	–97	dBm
Sensitivity for 1% packet error rate (PER) (+25 °C)	SENSper	—	–102		dBm
Saturation (maximum input level)	SENSmax	–10	—	—	dBm
Channel rejection for dual port mode (1% PER and desired signal –82 dBm)		—	39	—	dBm
+5 MHz (adjacent channel)		—	33	—	dBm
–5 MHz (adjacent channel)		—	50	—	dBm
+10 MHz (alternate channel)		—	50	—	dBm
–10 MHz (alternate channel)		—	58	—	dBm
>= 15 MHz					
Frequency error tolerance		—	—	200	kHz
Symbol rate error tolerance		80	—	—	ppm

Table 46. Transmitter AC electrical characteristics (V_{BAT}, V_{DDINT} = 2.7 V, T_A=25 °C, f_{ref} = 32 MHz unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power spectral density[1], absolute limit from –40°C to +105°C		–30	—	—	dBm
Power Spectral Density[2], Relative limit from –40°C to +105°C		–20	—	—	dB
Nominal output power[3]	Pout	–2	0	2	dBm
Maximum output power		—	8	—	dBm
Error vector magnitude	EVM	—	8	13	%
Output power control range[4]		—	40	—	dB
Over the air data rate		—	250	—	kbps
2nd harmonic[5]		—	<–50	<–40	dBm
3rd harmonic		—	<–50	<–40	dBm

1. [f-fc] > 3.5 MHz, average spectral power is measured in 100 kHz resolution BW.
2. For the relative limit, the reference level is the highest reference power measured within ±1 MHz of the carrier frequency.
3. Measurement is at the package pin.
4. Measurement is at the package pin on the output of the Tx/Rx switch. It does not degrade more than ±2 dB across temperature and an additional ±1 dB across all processes. Power adjustment will span nominally from –35 dBm to +8 dBm in 21 steps @ 2 dBm / step.
5. Measured with output power set to nominal (0 dBm) and temperature @ 25°C. Trap filter is needed.

Table 47. RF port impedance

Characteristic	Symbol	Typ	Unit
RFIN Pins for internal T/R switch configuration, TX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	 14.7 - j215 13.7 - j18.7 13 - j16.3	Ohm
RFIN Pins for internal or external T/R switch configuration, RX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	 14 - j9.5 13 - j7.6 12.3 - j5.6	Ohm

9.3 SPI timing: R_SSEL_B to R_SCLK

The following diagram describes timing constraints that must be guaranteed by the system designer.

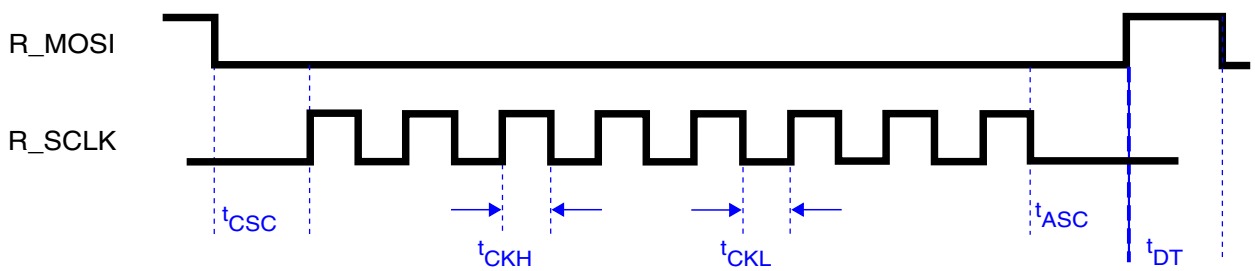


Figure 23. SPI timing: R_SSEL_B to R_SCLK

t_{CSC} (CS-to-SCK delay): 31.25 ns

t_{ASC} (After SCK delay): 31.25 ns

t_{DT} (Minimum CS idle time): 62.5 ns

t_{CKH} (Minimum R_SCLK high time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

t_{CKL} (Minimum R_SCLK low time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

Note

The SPI master device deasserts R_SSEL_B only on byte boundaries, and only after guaranteeing the t_{ASC} constraint shown above.

9.4 SPI timing: R_SCLK to R_MOSI and R_MISO

The following diagram describes timing constraints that must be guaranteed by the system designer. These constraints apply to the Master SPI (R_MOSI), and are guaranteed by the radio SPI (R_MISO).

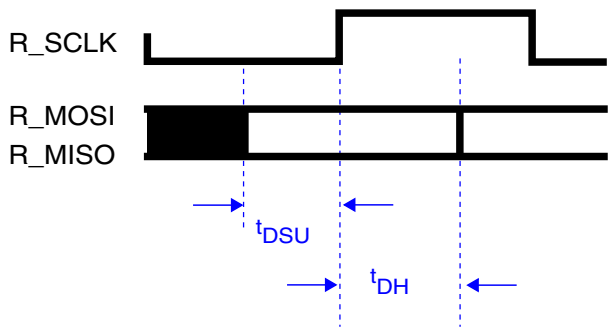


Figure 24. SPI timing: R_SCLK to R_MOSI and R_MISO

t_{DSU} (data-to-SCK setup): 10 ns

t_{DH} (SCK-to-data hold): 10 ns

10 Crystal oscillator reference frequency

This section provides application specific information regarding crystal oscillator reference design and recommended crystal usage.

10.1 Crystal oscillator design considerations

The IEEE ® 802.15.4 Standard requires that frequency tolerance be kept within ±40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The MKW2x transceiver provides on board crystal trim capacitors to assist in meeting this performance, while the bulk of the crystal load capacitance is external.

10.2 Crystal requirements

The suggested crystal specification for the MKW2x is shown in Table 48. A number of the stated parameters are related to desired package, desired temperature range and use of crystal capacitive load trimming.

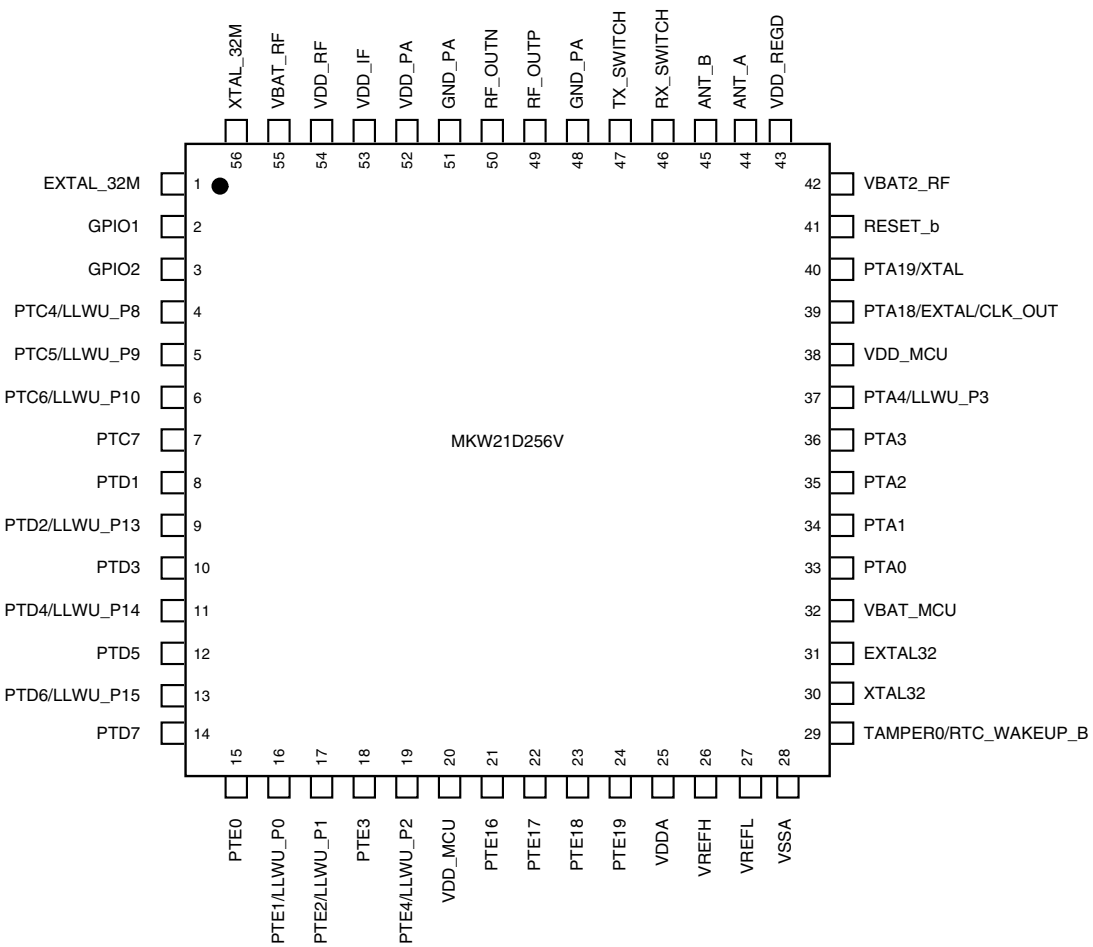
Table 48. MKW2x crystal specifications

Parameter	Value	Unit	Condition
Frequency	32	MHz	
Frequency tolerance (cut tolerance)	±10	ppm	at 25°C
Frequency stability (temperature)	±25	ppm	Over desired temperature range
Aging[1]	±2	ppm	max
Equivalent series resistance	60	Ω	max
Load capacitance	5–9	pF	
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

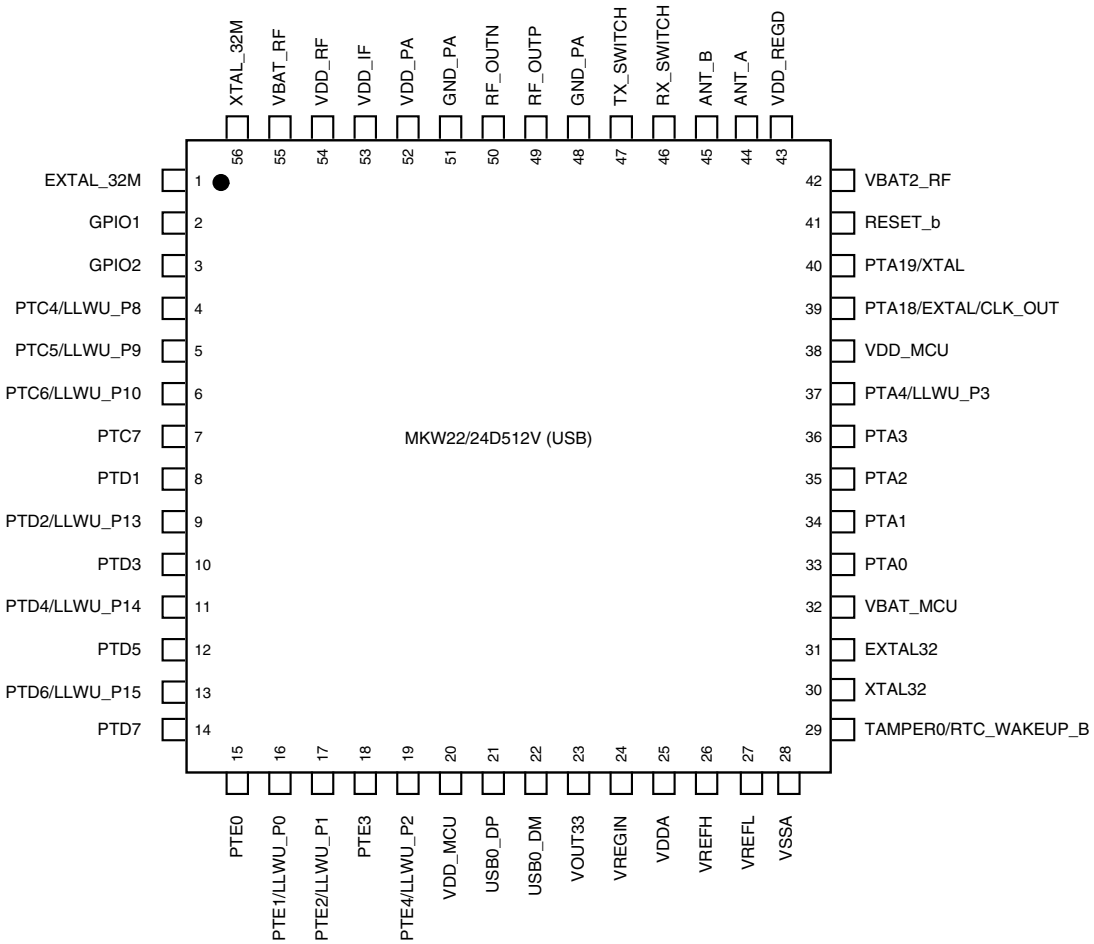
1. A wider aging tolerance may be acceptable if application uses trimming at production final test.

11 Pin diagrams and pin assignments

11.1 MKW21D256/MKW21D512 Pin Assignment



11.2 MKW22/24D512V Pin Assignment



11.3 Pin assignments

Note

SPI1 (ALT2): SPI1 is dedicated to the radio and is not an alternate MCU peripheral.

Table 49. Pin Assignments

MKW22/24D512 (USB)	MKW21D256/512	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
1	1	EXTAL_32M	EXTAL_32M									
2	2	GPIO1	GPIO1									
3	3	GPIO2	GPIO2									

Table continues on the next page...

Table 49. Pin Assignments (continued)

MKW22/24D512 (USB)	MKW21D256/512	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
4	4	PTC4/LLWU_P8	Disabled		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
5	5	PTC5/LLWU_P9	Disabled		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT		
6	6	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
7	7	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS				
8	8	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b					
9	9	PTD2/LLWU_P13	Disabled		PTD2/LLWU_P13	SPI0_SOUT	UART2_RX	I2C0_SCL				
10	10	PTD3	Disabled		PTD3	SPI0_SIN	UART2_TX	I2C0_SDA				
11	11	PTD4/LLWU_P14	ADC0_SE21	ADC0_SE21	PTD4/LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
12	12	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/UART0_COL_b	FTM0_CH5		EWM_OUT_b		
13	13	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
14	14	PTD7	ADC0_SE22	ADC0_SE22	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
15	15	PTE0	ADC0_SE10	ADC0_SE10	PTE0	SPI1_PCS1	UART1_TX		TRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT	
16	16	PTE1/LLWU_P0	DC0_SE11	ADC0_SE11	PTE1/LLWU_P0	SPI1_SOUT	UART1_RX		TRACE_D3	I2C1_SCL	SPI1_SIN	
17	17	PTE2/LLWU_P1	ADC0_DP1	ADC0_DP1	PTE2/LLWU_P1	SPI1_SCK	UART1_CTS_b		TRACE_D2			
18	18	PTE3	ADC0_DM1	ADC0_DM1	PTE3	SPI1_SIN	UART1_RTS_b		TRACE_D1		SPI1_SOUT	

Table continues on the next page...

Table 49. Pin Assignments (continued)

MKW22/24D512 (USB)	MKW21D256/512	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
19	19	PTE4/ LLWU_P2	Disabled		PTE4/ LLWU_P2	SPI1_PCS0			TRACE_D0			
20	20	VDD_MCU	VDD									
	21	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
	22	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
	23	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
	24	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
21		USB0_DP	USB0_DP	USB0_DP								
22		USB0_DM	USB0_DM	USB0_DM								
23		VOUT33	VOUT33	VOUT33								
24		VREGIN	VREGIN	VREGIN								
25	25	VDDA	VDDA	VDDA								
26	26	VREFH	VREFH	VREFH								
27	27	VREFL	VREFL	VREFL								
28	28	VSSA	VSSA	VSSA								
29	29	TAMPER0/ RTC_WAKEUP_B	TAMPER0/ RTC_WAKEUP_B	TAMPER0/ RTC_WAKEUP_B								
30	30	XTAL32	XTAL32	XTAL32								
31	31	EXTAL32	EXTAL32	EXTAL32								
32	32	VBAT_MCU	VBAT_MCU	VBAT_MCU								
33	33	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK

Table continues on the next page...

Table 49. Pin Assignments (continued)

MKW22/24D512 (USB)	MKW21D256/512	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
34	34	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
35	35	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
36	36	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
37	37	PTA4/ LLWU_P3	NMI_b/EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
38	38	VDD2_MCU	VDD	VDD								
39	39	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
40	40	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
41	41	RESET_b	RESET_b	RESET_b								
42	42	VBAT2_RF	VBAT2_RF									
43[1]	43[1]	VDD_REGD	VDD_REGD									
44	44	ANT_A	ANT_A									
45	45	ANT_B	ANT_B									
46	46	RX_SWITCH	RX_SWITCH									
47	47	TX_SWITCH	TX_SWITCH									
48	48	GND_PA	VSSA_PA									
49	49	RF_OUTP	RF_OUTP									
50	50	RF_OUTN	RF_OUTN									
51	51	GND_PA	VSSA_PA									
52[1]	52[1]	VDD_PA	VDD_PA									
53[1]	53[1]	VDD_IF	VDD_IF									

Table continues on the next page...

Table 49. Pin Assignments (continued)

MKW22/24D512 (USB)	MKW21D256/512	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
54[1]	54[1]	VDD_RF	VDD_RF									
55	55	VBAT_RF	VBAT									
56	56	XTAL_32M	XTAL_32M									
57	57	Factory test	Do not connect									
58	58	Factory test	Do not connect									
59	59	Factory test	Do not connect									
60	60	Factory test	Do not connect									
61	61	Factory test	Do not connect									
62	62	Factory test	Do not connect									
63	63	GND_PA	Connect to ground									

1. This pin is used for external bypassing of an internal regulator. DO NOT connect to power.

12 Dimensions

12.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
63 MAPLGA	98ASA00393D

How to Reach Us:

Home Page:
freescale.com

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freescale.com/support

Document Number: MKW2xDxxx
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11/2013