PIC18(L)F6XK40

PIC18(L)F6XK40 Memory Programming Specification

1.0   OVERVIEW

This programming specification describes an SPI-based programming method for the PIC18(L)F6XK40 family of microcontrollers. **Section 3.0 "Programming Algorithms"** describes the programming commands, programming algorithms and electrical specifications which are used in that particular programming method. **Appendix B** contains individual part numbers, device identification and checksum values, pinout and packaging information, and Configuration Words.

Note 1:	This is a SPI-compatible programming method with 8-bit commands.
2:	The low-voltage entry code is now 32 clocks and MSb first, unlike previous PIC18 devices which had 33 clocks and LSb first.

1.1   Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage In-Circuit Serial Programming (ICSP) interface. Data can be programmed into the Program Flash Memory (PFM), Data EEPROM Memory, dedicated "User ID" locations and the Configuration Words.

1.2   Write and/or Erase Selection

Erasing or writing is selected according to the command used to begin operation (see Table 3-1). The terminologies used in this document, related to erasing/writing to the program memory, are defined in Table 1-1 and are detailed below.

TABLE 1-1:   PROGRAMMING TERMS

Term	Definition
Programmed Cell	A memory cell at logic '0'
Erased Cell	A memory cell at logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic erase and/or write

1.2.1   ERASING MEMORY

Memory is erased by row or in bulk, where 'bulk' includes many subsets of the total memory space. The duration of the erase is determined by the size of program memory. All Bulk ICSP Erase commands have minimum V_{DD} requirements, which are higher than the Row Erase and write requirements.

1.2.2   WRITING MEMORY

Memory is written one row at a time. Multiple load data for NVM commands is used to fill the row data latches. The duration of the write can be determined either internally or externally.

1.2.3   MULTI-WORD PROGRAMMING INTERFACE

Program Flash Memory (PFM) panels include up to a 64-word (one row) programming interface. Refer to Table 3-3 for row size of erase and write operations for the PIC18(L)F6XK40 family. The row to be programmed must first be erased, either with a Bulk Erase or a Row Erase.

1.3 Hardware Requirements

1.3.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for V_{DD} and one for the $\overline{MCLR}$/V_{PP} pin.

1.3.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, the device can be programmed using a single V_{DD} source in the operating range. The $\overline{MCLR}$/V_{PP} pin does not have to be brought to programming voltage, but can instead be left at the normal operating voltage.

1.3.2.1 Single-Supply ICSP Programming

The device's LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled). The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the $\overline{MCLR}$/V_{PP} pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

> **Note 1:** The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}$/V_{PP} pin.
>
> **2:** While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled, regardless of the MCLRE bit. Also, the port pin can no longer be used as a general purpose input.

1.4 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in Table 1-2. For pin locations and packaging information, please refer to Table B-3.

TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ICSPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ICSPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{MCLR}$/V_{PP}	Program/Verify mode	I[1]	Program Mode Select
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

2.0   MEMORY MAP

TABLE 2-1:   **PROGRAM AND DATA EEPROM MEMORY MAP**

	PIC18(L)F65K40	PIC18(L)F66K40	PIC18(L)F67K40	
	PC<21:0>	PC<21:0>	PC<21:0>	
Note 1	Stack (31 levels)	Stack (31 levels)	Stack (31 levels)	**Note 1**
00 0000h	Reset Vector	Reset Vector	Reset Vector	00 0000h
• • •	• • •	• • •	• • •	• • •
00 0008h	Interrupt Vector High	Interrupt Vector High	Interrupt Vector High	00 0008h
• • •	• • •	• • •	• • •	• • •
00 0018h	Interrupt Vector Low	Interrupt Vector Low	Interrupt Vector Low	00 0018h
00 001Ah				00 001Ah
00 3FFFh	Program Flash Memory (16 KW)			00 3FFFh
00 4000h		Program Flash Memory (32 KW)		00 4000h
00 7FFFh				00 7FFFh
00 8000h			Program Flash Memory (64 KW)	00 8000h
00 FFFFh				00 FFFFh
01 0000h	Not present(2)			01 0000h
01 FFFFh		Not present(2)		01 FFFFh
02 0000h			Not present(2)	02 0000h
1F FFFFh				1F FFFFh
20 0000h	User IDs (8 Words)(3)			20 0000h
• • •				• • •
20 000Fh				20 000Fh
20 0010h	Reserved			20 0010h
• • •				• • •
2F FFFFh				2F FFFFh
30 0000h	Configuration Words (6 Words)(3)			30 0000h
• • •				• • •
30 000Bh				30 000Bh
30 000Ch	Reserved			30 000Ch
• • •				• • •
30 FFFFh				30 FFFFh
31 0000h	DataEEByte0 • • • DataEEByte1023			31 0000h
• • •				• • •
31 00FFh				
• • •				• • •
31 03FFh				31 03FFh
31 0400h	Reserved			31 0400h
• • •				• • •
3F FFFBh				3F FFFBh
3F FFFCh	Revision ID (1 Word)(4)			3F FFFCh
• • •				• • •
3F FFFDh				3F FFFDh
3F FFFEh	Device ID (1 Word)(4)			3F FFFEh
• • •				• • •
3F FFFFh				3F FFFFh

Note 1:   The stack is a separate SRAM panel, apart from all user memory panels.
   2:   The addresses do not roll over. The region is read as '0'.
   3:   Not code-protected.
   4:   Device/Revision IDs are hard-coded in silicon.

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TABLE 2-2: MEMORY MAP AND CODE PROTECTION CONTROL

Reg.	Address (from/to)	Device		
		PIC18(L)F65K40	PIC18(L)F66K40	PIC18(L)F67K40
PFM	00 0000h – 00 07FFh	Boot Block 1 KW CP, WRTB, EBTRB	Boot Block 1 KW CP WRTB, EBTRB	Boot Block 1 KW CP WRTB, EBTRB
	00 0800h – 00 1FFFh	Block 0 3 KW CP, WRT0, EBTR0	Block 0 7 KW CP, WRT0, EBTR0	Block 0 7 KW CP, WRT0, EBTR0
	00 2000h – 00 3FFFh	Block 1 4 KW CP, WRT1, EBTR1		
	00 4000h – 00 5FFFh	Block 2 4 KW CP, WRT2, EBTR2	Block 1 8 KW CP, WRT1, EBTR1	Block 1 8 KW CP, WRT1, EBTR1
	00 6000h – 00 7FFFh	Block 3 4 KW CP, WRT3, EBTR3		
	00 8000h – 00 BFFFh	Not present	Block 2 8 KW CP, WRT2, EBTR2	Block 2 8 KW CP, WRT2, EBTR2
	00 C000h – 00 FFFFh		Block 3 8 KW CP, WRT3, EBTR3	Block 3 8 KW CP, WRT3, EBTR3
	01 0000h – 01 3FFFh		Not present	Block 4 8 KW CP, WRT4, EBTR4
	01 4000h – 01 7FFFh			Block 5 8 KW CP, WRT5, EBTR5
	01 8000h – 01 BFFFh			Block 6 8 KW CP, WRT6, EBTR6
	01 C000h – 01 FFFFh			Block 7 8 KW CP, WRT7, EBTR7
CONFIG	30 0000h – 30 000Bh	6 Words WRTC		
Data EEPROM	31 0000h 31 00FFh 31 0100h 31 03FFh	1 KW CPD, WRTD		

2.1 User ID Location

A user may store identification information (User ID) in eight designated locations. The User ID locations are mapped to 20 0000h-20 000Fh. Each location is 16 bits in length. It is recommended that the Most Significant nibble of each ID be Fh. In doing so, if the user code inadvertently tries to execute from the ID space, the ID data will execute as a `NOP`. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

2.2 Device/Revision ID

The 16-bit Device ID Word is located at 3F FFFEh and the 16-bit Revision ID is located at 3F FFFCh. These locations are read-only and cannot be erased or modified.

REGISTER 2-1: DEVICEID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
DEV15	DEV14	DEV13	DEV12	DEV11	DEV10	DEV9	DEV8
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DEV<15:0>:** Device ID bits

REGISTER 2-2: REVISIONID: REVISION ID REGISTER

R	R	R	R	R	R	R	R
1	0	1	0	MJRREV<5:2>			
bit 15							bit 8

R	R	R	R	R	R	R	R
MJRREV<1:0>		MNRREV<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Read as '1010'**

These bits are fixed with value, '1010', for all devices in this programming specification.

bit 11-6 **MJRREV<5:0>:** Major Revision ID bits

These bits are used to identify a major revision. A major revision is indicated by an all layer revision (A0, B0, C0, etc...).
Revision A = 6'b00_0000

bit 5-0 **MNRREV<5:0>:** Minor Revision ID bits

These bits are used to identify a minor revision.
Revision A0 = 6'b00_0000

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2.3 Configuration Words

The devices have six Configuration Words starting at address, 30 0000h. The individual bits within these Configuration Words are critical to the correct operation of the system. Configuration bits enable or disable specific features, placing these controls outside the normal software process, and they establish configured values prior to the execution of any software.

In terms of programming, these important Configuration bits should be considered:

1. **LVP: Low-Voltage Programming Enable bit**

    1 = ON – Low-Voltage Programming is enabled. $\overline{\text{MCLR}}$/V$_{PP}$ pin function is $\overline{\text{MCLR}}$.
    MCLRE Configuration bit is ignored.

    0 = OFF – High Voltage on $\overline{\text{MCLR}}$/V$_{PP}$ must be used for programming.

It is important to note that the LVP bit cannot be written (to '0') while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the configuration state. For more information, see **Section 3.1.2 "Low-Voltage Programming (LVP) Mode"**.

2. **MCLRE: Master Clear ($\overline{\text{MCLR}}$) Enable bit**

- If LVP = 1

    RE3 pin function is $\overline{\text{MCLR}}$

- If LVP = 0

    1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
    0 = $\overline{\text{MCLR}}$ pin function is a port defined function

3. **$\overline{\text{CPD}}$: Data NVM (EEPROM) Memory Code Protection bit**

    1 = OFF – Data NVM code protection is disabled
    0 = ON   – Data NVM code protection is enabled

4. **$\overline{\text{CP}}$: User NVM Program Memory Code Protection bit**

    1 = OFF – User NVM code protection is disabled
    0 = ON   – User NVM code protection is enabled

For more information on code protection, see **Section 3.3 "Code Protection"**.

3.0   PROGRAMMING ALGORITHMS

3.1   Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

3.1.1   HIGH-VOLTAGE PROGRAM/VERIFY MODE ENTRY AND EXIT

There are two different modes of entering Program/Verify mode via high voltage:

- V$_{PP}$ – First Entry mode
- V$_{DD}$ – First Entry mode

3.1.1.1   V$_{PP}$ – First Entry Mode

To enter Program/Verify mode via the V$_{PP}$-First mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V$_{IHH}$.
3. Raise the voltage on V$_{DD}$ from 0V to the desired operating voltage.

The V$_{PP}$-First entry prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has already been programmed to have $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer disabled ($\overline{PWRTE}$ = 0) and the internal oscillator selected, the device will execute code immediately. Since this may prevent entry, V$_{PP}$-First Entry mode is strongly recommended as it prevents user code from changing EEPROM contents or driving pins to affect Program/Verify mode entry. See the timing diagram in Figure 3-1.

3.1.1.2   V$_{DD}$ – First Entry Mode

To enter Program/Verify mode via the V$_{DD}$-First mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on V$_{DD}$ from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V$_{DD}$ or below to V$_{IHH}$.

The V$_{DD}$-First mode is useful for programming the device when V$_{DD}$ is already applied, for it is not necessary to disconnect V$_{DD}$ to enter Program/Verify mode. See the timing diagram in Figure 3-2.

3.1.1.3   Program/Verify Mode Exit

To exit Program/Verify mode, lower $\overline{MCLR}$ from V$_{IHH}$ or lower (V$_{IL}$). V$_{PP}$-First Entry mode should use V$_{PP}$-Last Exit mode (see Figure 3-1). V$_{DD}$-First Entry mode should use V$_{DD}$-Last Exit mode (see Figure 3-2).

FIGURE 3-1: **PROGRAMMING ENTRY AND EXIT MODES – VPP-FIRST AND LAST**

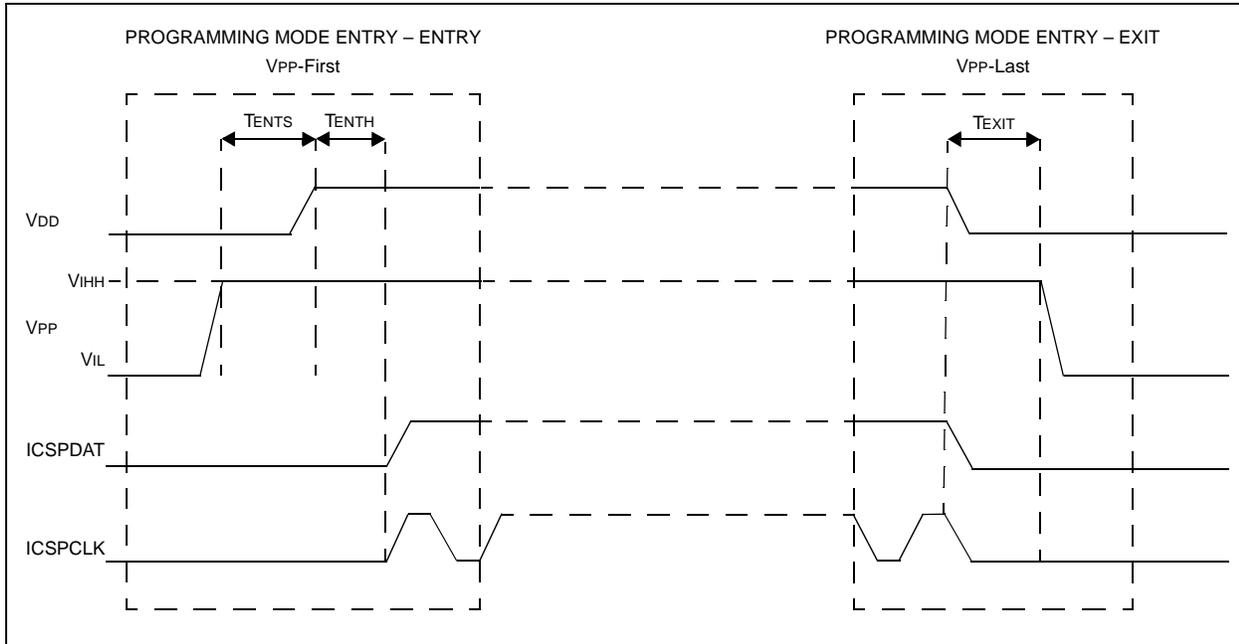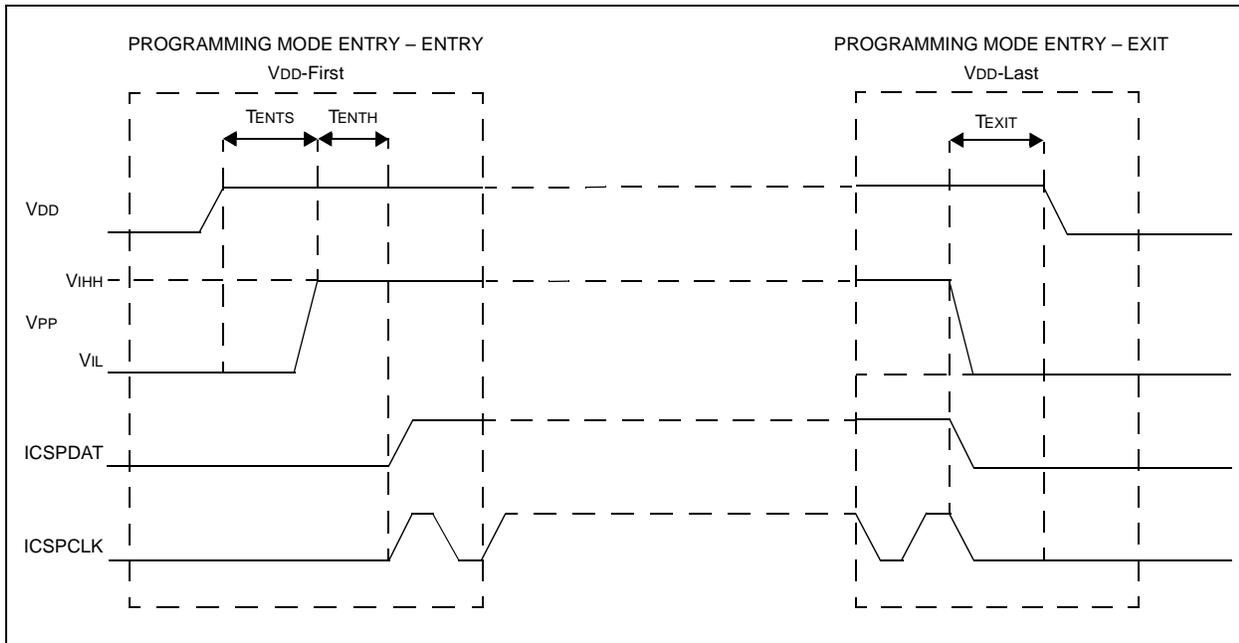**FIGURE 3-2:** **PROGRAMMING ENTRY AND EXIT MODES – VDD-FIRST AND LAST**

3.1.2 LOW-VOLTAGE PROGRAMMING (LVP) MODE

The Low-Voltage Programming mode allows the devices to be programmed using V$_{DD}$ only, without high voltage. When the LVP bit of the Configuration Word 3 register is set to '1', the Low-Voltage ICSP Programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to V$_{IL}$.
2. A **32-bit key sequence** is presented on ICSPDAT. The LSb of the pattern is a "don't care x". The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required before the pattern detect goes active.

The key sequence is a specific 32-bit pattern, '32'h4d434850' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the Most Significant nibble must be shifted in first. Once the key sequence is complete, $\overline{MCLR}$ must be held at V$_{IL}$ for as long as Program/Verify mode is to be maintained. For LVP timing, see Figure 3-3 and Figure 3-4.

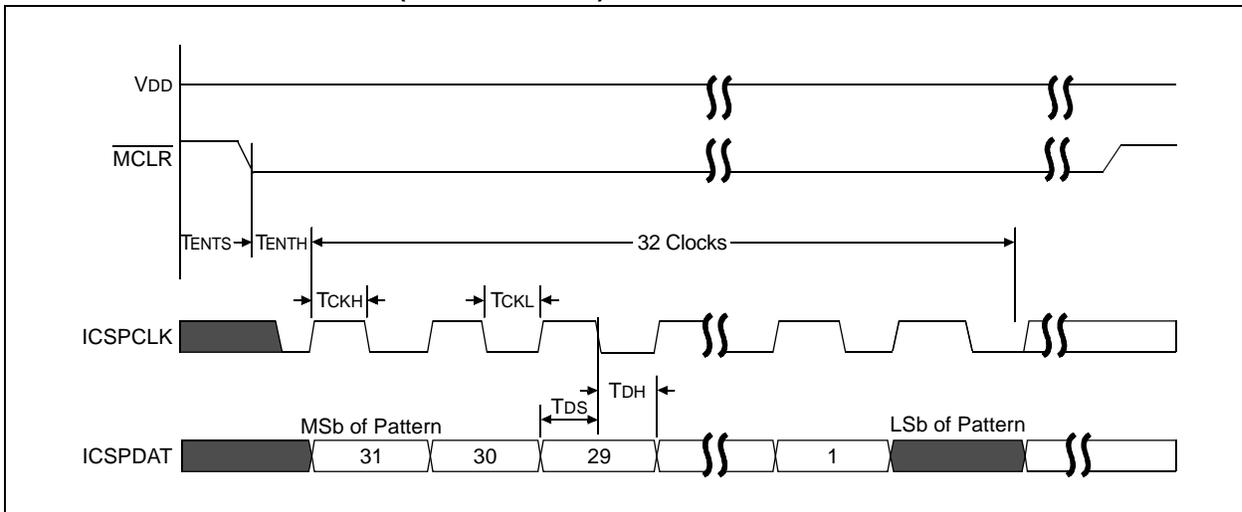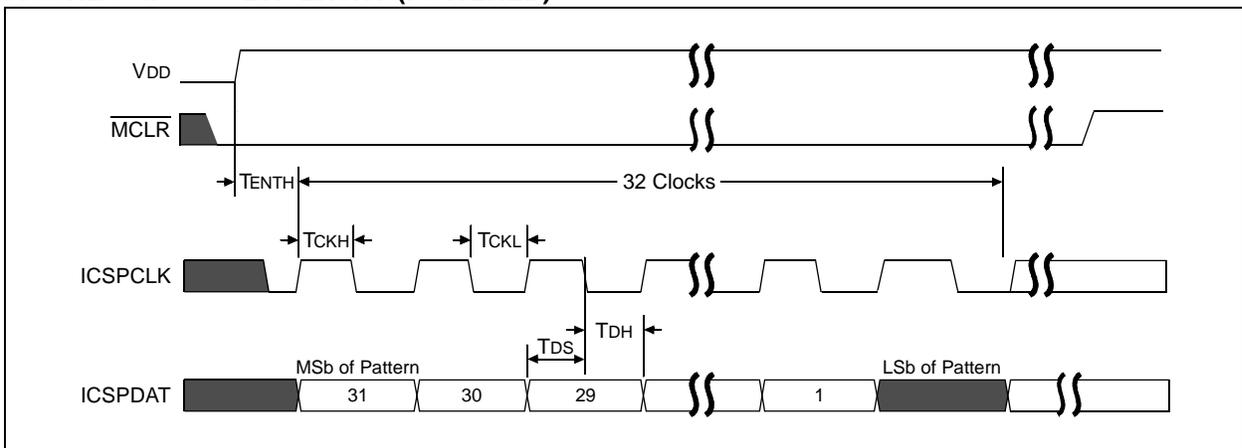**FIGURE 3-3: LVP ENTRY (POWERING UP)**

FIGURE 3-4: LVP ENTRY (POWERED)

Exiting Program/Verify mode is done by raising $\overline{MCLR}$ from below V$_{IL}$ to V$_{IH}$ level (or higher, up to V$_{DD}$).

> **Note:** To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

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3.1.3   PROGRAM/VERIFY COMMANDS

Once a device has entered ICSP Program/Verify mode (using either high-voltage or LVP entry), the programming host device may issue nine commands to the microcontroller, each eight bits in length. The commands are summarized in Table 3-1. The commands are used to erase or program the device based on the location of the Program Counter (PC).

Some of the 8-bit commands also have a data payload associated with it (such as Load Data for NVM and Read Data from NVM).

If the programming host device issues an 8-bit command byte that has a data payload associated with it, the host device is responsible for sending an additional 24 clock pulses (for example, three 8-bit bytes) in order to send or receive the payload data associated with the command.

The payload field size is used so as to be compatible with many 8-bit SPI-based systems. Within each 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad bits, followed by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted Most Significant bit (MSb) first.

When the programming device issues a command that involves a host to microcontroller payload (for example, Load PC Address), the Start, Stop and Pad bits should all be driven by the programmer to '0'. When the programming host device issues a command that involves microcontroller to host payload data (for example, Read Data from NVM), the Start, Stop and Pad bits should be treated as "don't care" bits and the values should be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host should wait a minimum amount of delay (which is command-specific) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

TABLE 3-1:   ICSP™ COMMAND SET SUMMARY

| Command Name | Command Value | | Payload Expected | Delay after Command | Data/Note |
	Binary (MSb … LSb)	Hex			
Load PC Address	`1000 0000`	80	Yes	T_{DLY}	Payload value = PC
Bulk Erase Program Memory	`0001 1000`	18	No	T_{ERAB}	Depending on the current value of the PC, one or more memory regions.
Row Erase Program Memory	`1111 0000`	F0	No	T_{ERAR}	The row addressed by the MSbs of the PC is erased; LSbs are ignored.
Load Data for NVM	`0000 00J0`	00/02	Yes	T_{DLY}	Data is loaded to the data latch addressed by the PC; J = 0: PC is unchanged J = 1: PC = PC + 2 after writing
Read Data from NVM	`1111 11J0`	FC/FE	Yes	T_{DLY}	Data output '0' if code-protect is enabled; J = 0: PC is unchanged J = 1: PC = PC + 2 after reading
Increment Address	`1111 1000`	F8	No	T_{DLY}	PC = PC + 2
Begin Internally Timed Programming	`1110 0000`	E0	No	T_{PINT}	Commits latched data to NVM (self-timed).
Begin Externally Timed Programming	`1100 0000`	C0	No	T_{PEXT}	Commits latched data to NVM (externally timed). After T_{PEXT}, "End Externally Timed Programming" command must be issued.
End Externally Timed Programming	`1000 0010`	82	No	T_{DIS}	Should be issued within required time delay (T_{PEXT}) after "Begin Externally Timed Programming" command.

> **Note:** All clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller should latch received ICSPDAT values on the falling edge of the ICSPCLK line. When the microcontroller receives ICSPDAT line values from the host programmer, the ICSPDAT values must be valid a minimum of T_{DS} before the falling edges of ICSPCLK and should remain valid for a minimum of T_{DH} after the falling edge of ICSPDAT. See Figure 3-5.

FIGURE 3-5: **CLOCK AND DATA TIMING**
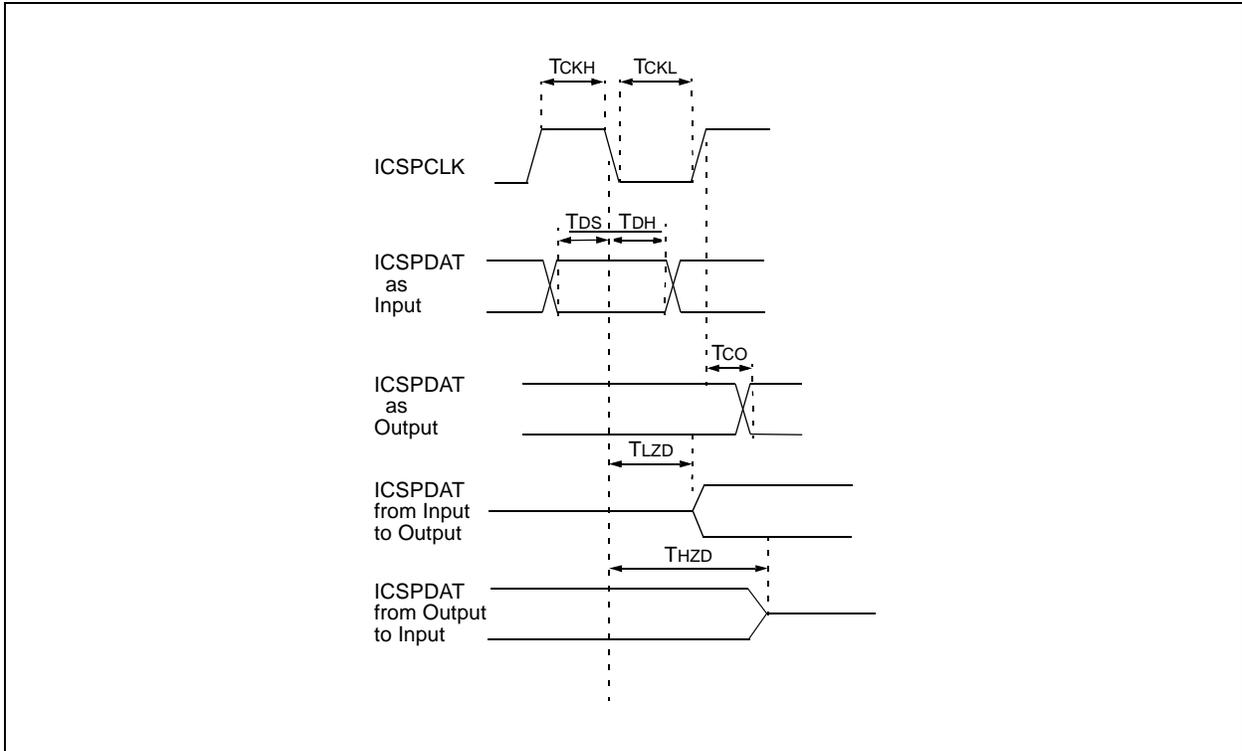
3.1.3.1   Load Data for NVM

The Load Data for NVM command is used to load one programming data latch (for example, one 16-bit instruction word for program memory/configuration memory/User ID memory or one 8-bit data for a Data EEPROM Memory address). The latched data is written into program or EEPROM memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see **Section 3.2 "Programming Algorithms"**). The Load Data for the NVM command can be used to load data for Program Flash Memory (PFM) (see Figure 3-6) or the Data EEPROM Memory (see Figure 3-7). Depending on the value of bit 1 of the command, the PC may or may not be incremented (see Table 3-1).

FIGURE 3-6:   LOAD DATA FOR NVM (PFM)
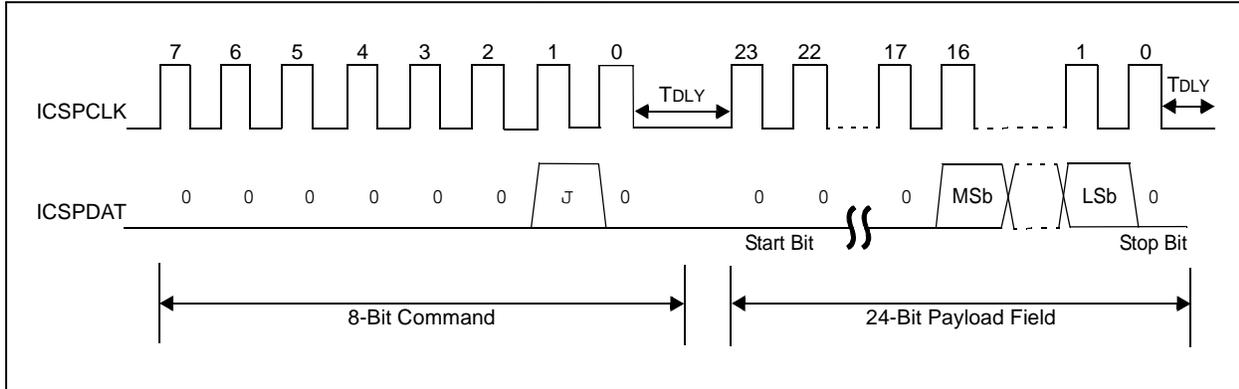
FIGURE 3-7:   LOAD DATA FOR NVM (DATA EEPROM)
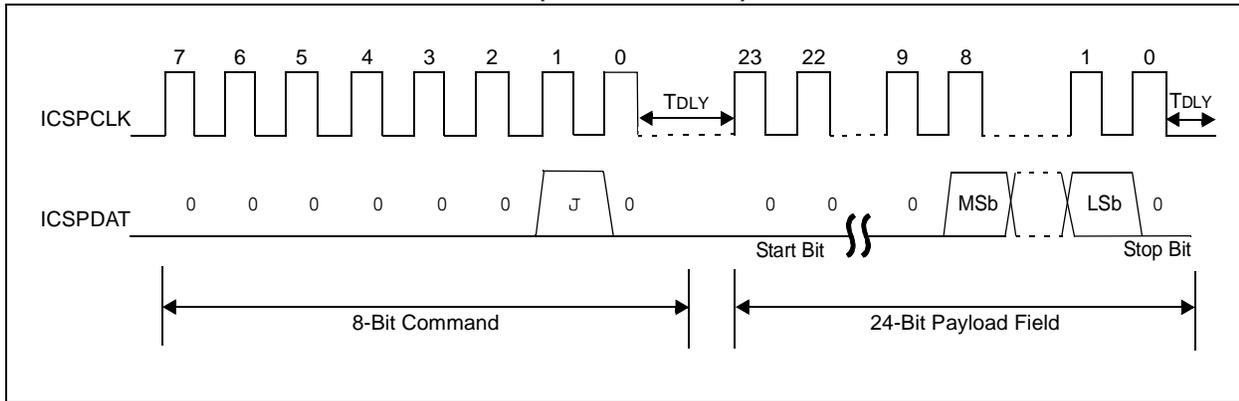
3.1.3.2 Read Data from NVM

The Read Data from NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of the ICSP data payload clock and it will revert to Input mode (high-impedance) after the 24th falling edge of the ICSP data payload clock. The Start and Stop bits are only one-half-of-a-bit-time wide; therefore, they should be ignored by the host programmer device, since the latched value may be indeterminate. Additionally, the host programmer device should only consider the MSb to LSb payload bits as valid and should ignore the values of the Pad bits. If the program memory is code-protected (CP), the data will be read as zeros (see Figure 3-8 and Figure 3-9). Depending on the value of bit<1> of the command, the PC may or may not be incremented (see Table 3-1). The Read Data for NVM command can be used to read data for Program Flash Memory (PFM) (see Figure 3-8) or the Data EEPROM Memory (see Figure 3-9).

FIGURE 3-8: **READ DATA FROM NVM (PFM OR CONFIGURATION WORDS)**
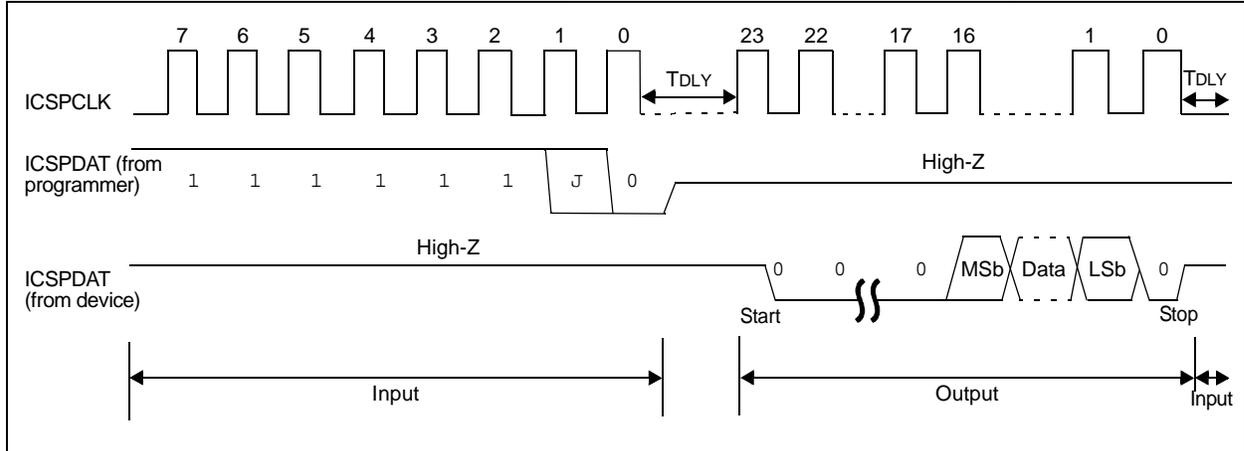
FIGURE 3-9: **READ DATA FROM NVM (DATA EEPROM)**
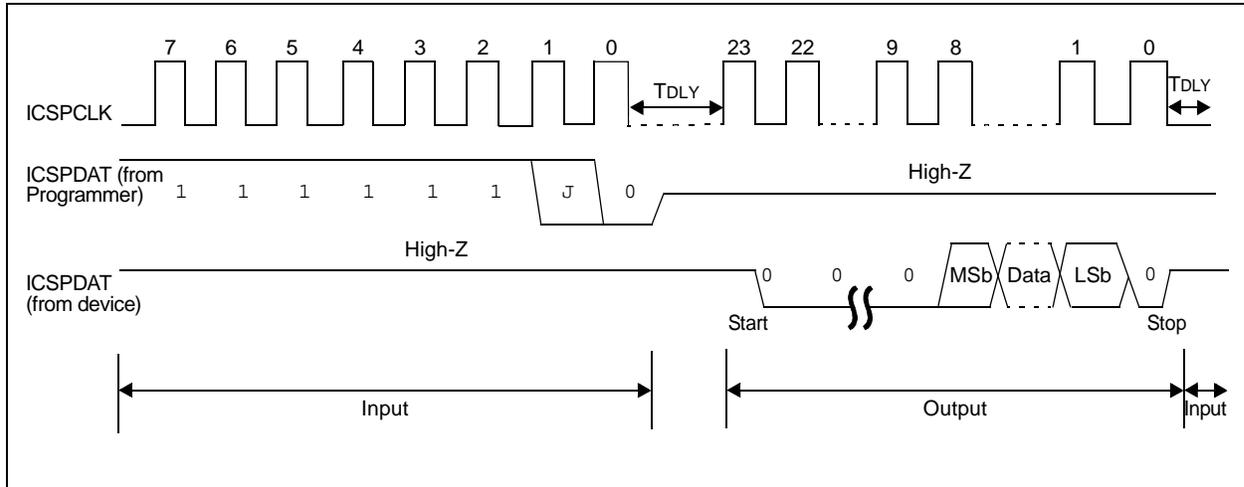
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3.1.3.3   Increment Address

The address is incremented when this command is received. Depending on the current value of the Program Counter, the increment varies. If the PC points to PFM, then the PC is incremented by two; if the PC points to data EEPROM, then it is incremented by one. It is not possible to decrement the address. To reset this counter, the user must use the Load PC Address command.

FIGURE 3-10:   INCREMENT ADDRESS
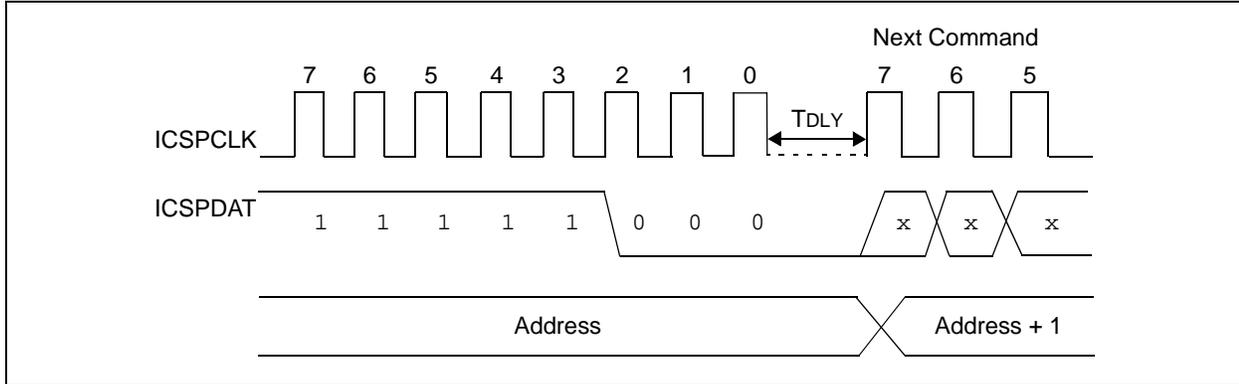
3.1.3.4   Load PC Address

The PC value is set using the supplied data. The address implies the memory panel (PFM or Data EEPROM Memory) to be accessed (see Figure 3-11).

FIGURE 3-11:   LOAD PC ADDRESS
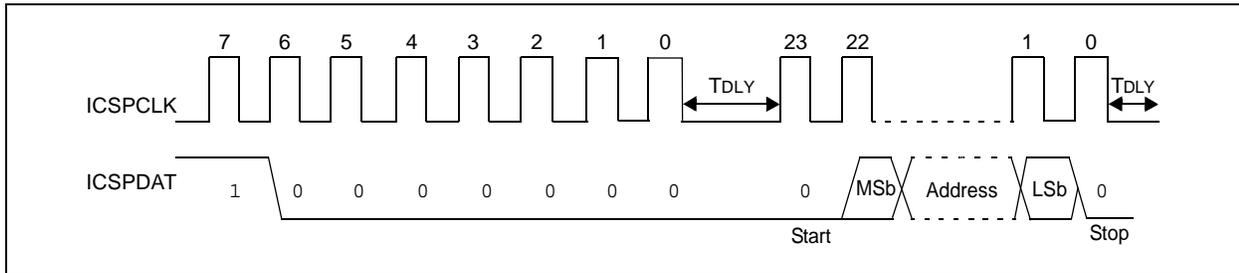
3.1.3.5   Begin Internally Timed Programming

The write programming latches must already have been loaded using the Write Data for NVM command, prior to issuing the Begin Programming command (see **Section 3.2 "Programming Algorithms"**). Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the erase/write cycle time, T_{PINT}, in order for the programming to complete, prior to issuing the next command byte (see Figure 3-12).

After the programming cycle is complete, all of the data latches are reset to '1'. The command is ignored when the fuse latched values of CP == 0 or CPD == 0 (i.e., if either device memory is currently protected).

FIGURE 3-12:   BEGIN INTERNALLY TIMED PROGRAMMING
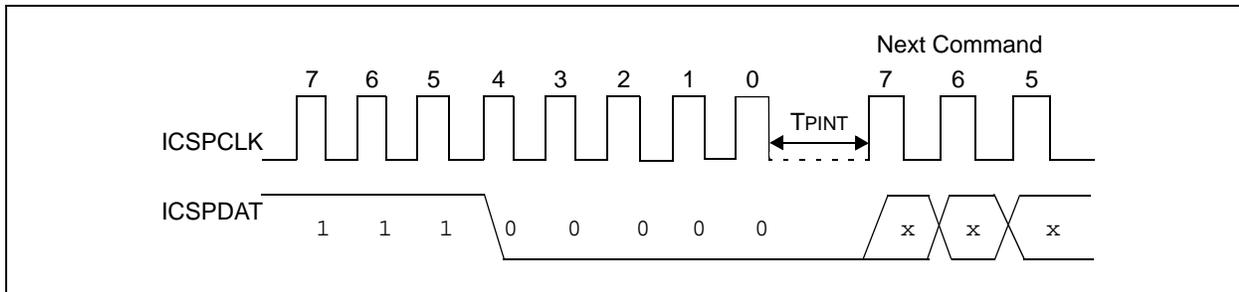
3.1.3.6 Begin Externally Timed Programming

Data to be programmed must be previously loaded by the Load Data for NVM command before every Begin Programming command. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT (see Figure 3-13).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 3-13: BEGIN EXTERNALLY TIMED PROGRAMMING
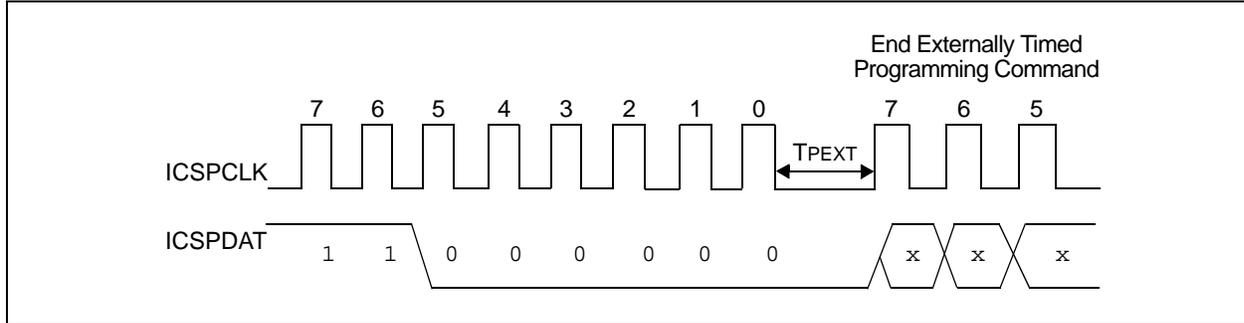
3.1.3.7 End Externally Timed Programming

This command is required to terminate the programming sequence after a Begin Externally Timed Programming command is given. If no programming command is in progress, or if the programming cycle is internally timed, this command will execute as a No Operation (NOP) (see Figure 3-14).

FIGURE 3-14: END EXTERNALLY TIMED PROGRAMMING
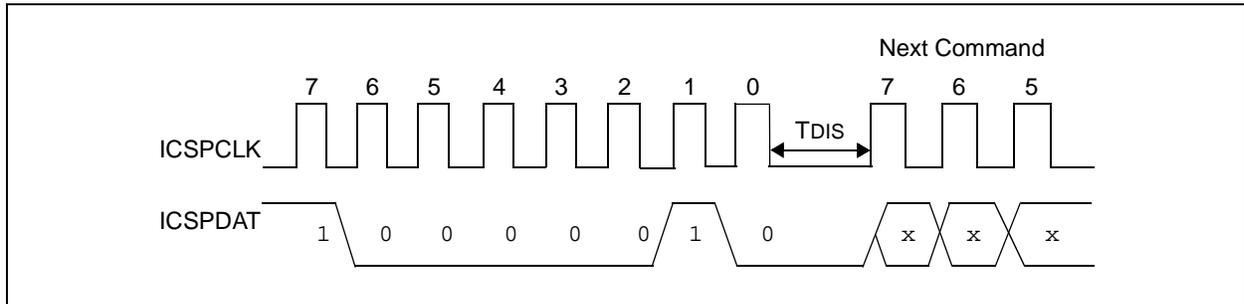
3.1.3.8 Bulk Erase Memory

The Bulk Erase command affects specific portions of the memory depending on the initial value of the Program Counter. Whenever a Bulk Erase command is executed, the device will erase all bytes within the regions listed in Table 3-2.

TABLE 3-2:   BULK ERASE

Address	Area(s) Erased	
	$\overline{\text{CP}}$ = x and $\overline{\text{CPD}}$ = 1 (both disabled)	$\overline{\text{CP}}$ = x or $\overline{\text{CPD}}$ = 0 (either enabled)
00 0000h-01 FFFFh	Program Flash Memory Configuration Words	Program Flash Memory Data EEPROM Configuration Words
30 0000h-30 001Fh	Program Flash Memory User ID Words Configuration Words	Program Flash Memory Data EEPROM User ID Words Configuration Words
31 0000h-3F FFFFh	Data EEPROM Only	Data EEPROM Only

After receiving the Bulk Erase Memory command, the erase will not complete until the time interval, T_{ERAB}, has expired (see Figure 3-15). The programming host device should not issue another 8-bit command until after the T_{ERAB} interval has fully elapsed.

FIGURE 3-15:   BULK ERASE MEMORY
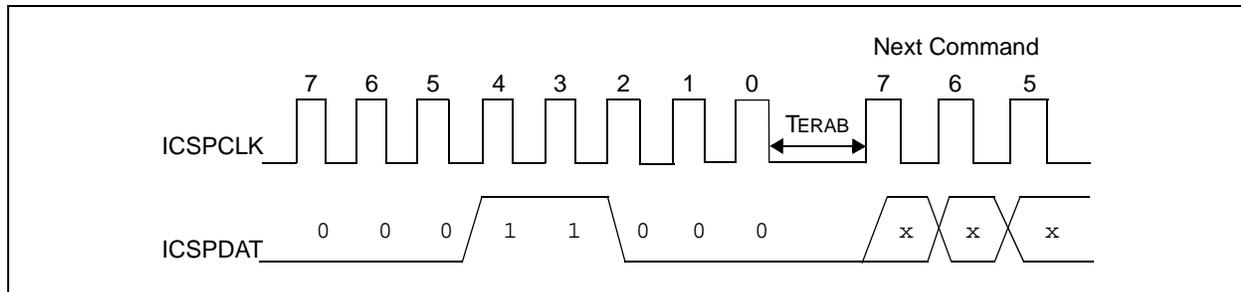
3.1.3.9 Row Erase Memory

The Row Erase Memory command will erase an individual row based on the current address of the Program Counter.

Write and erase operations are done on a row basis. Refer to Table 3-3 for row size of erase and write operations for other devices in the PIC18(L)F6XK40 family. For example, in the PIC18(L)F65K40 device, the row size (number of 16-bit words) for write/erase operation is 32, and the write latches per row (number of 8-bit latches) required for the write/erase operation is 64. If the program memory is code-protected, the Row Erase Program Memory command will be ignored.

The Flash memory row defined by the current PC will be erased. The user must wait T_{ERAR} for erasing to complete (see Figure 3-16).

TABLE 3-3: PROGRAM MEMORY ROW SIZES

Variant	Row Size (words)	Byte-Wide Write Latches per Row
PIC18(L)F65K40	32	64
PIC18(L)F66K40	32	64
PIC18(L)F67K40	64	128

FIGURE 3-16: ROW ERASE MEMORY
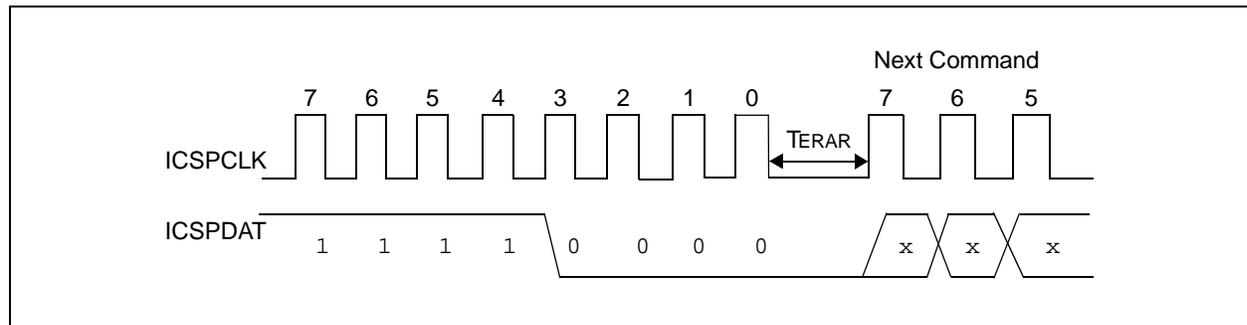
3.2 Programming Algorithms

The devices use internal latches to temporarily store the 16-bit words used for programming. The data latches allow the user to write the program words with a single Begin Internally Timed Programming or Begin Externally Timed Programming command. The Load Data for NVM command is used to load a single data latch. The data latch will hold the data until the Begin Internally Timed Programming or Begin Externally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The address used at the time the Begin Internally Timed Programming or Begin Externally Timed Programming command is given will determine which memory row is written. Writes cannot cross a physical row boundary. For example, attempting to write from address, 0002h-0021h, in a 32-latch device will result in data being written to 0020h-003Fh.

If more than the maximum number of latches is written without a Begin Internally Timed Programming or Begin Externally Timed Programming command, the data in the data latches will be overwritten. Figure 3-17 through Figure 3-22 show the recommended flowcharts for programming.

> **Note:** The Program Flash Memory regions are programmed one row at a time (Figure 3-18), while the User ID and Configuration Words are programmed one word at a time (Figure 3-19). The EEPROM memory is programmed one byte at a time. Refer to Table 3-3 for row size.
>
> The value of the PC at the time of issuing the Begin Internally Timed Programming command determines what row (of Program Flash Memory or EEPROM) or what word (of User ID or Configuration Word) will get programmed.

FIGURE 3-17: **DEVICE PROGRAM/VERIFY FLOWCHART**

```
                    ( Start )
                        │
                        ▼
              ┌──────────────────┐
              │      Enter       │
              │ Programming Mode │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │    Bulk Erase    │
              │      Device      │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │  Write Program   │
              │   Memory(1)      │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │  Verify Program  │
              │      Memory      │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │ Write Data EEPROM│
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │   Verify Data    │
              │  EEPROM Memory   │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │  Write User IDs  │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │ Verify User IDs  │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │Write Configuration│
              │   Words(2)       │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │Verify Configuration│
              │      Words       │
              └──────────────────┘
                        │
                        ▼
              ┌──────────────────┐
              │ Exit Programming │
              │       Mode       │
              └──────────────────┘
                        │
                        ▼
                    ( Done )
```

Note 1: See Figure 3-18.
2: See Figure 3-21.
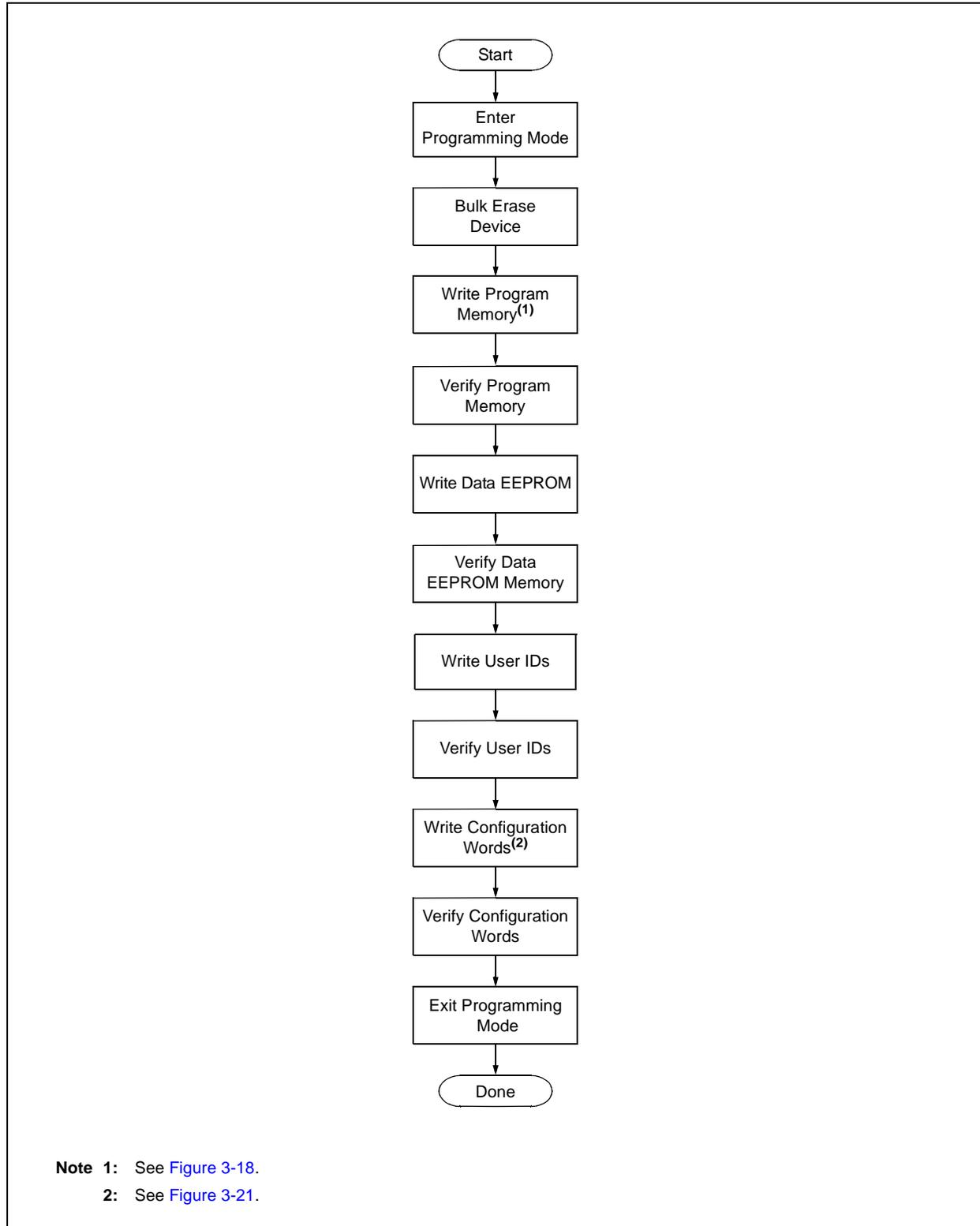
FIGURE 3-18: **PROGRAM MEMORY FLOWCHART**

Start

Bulk Erase
Program
Memory[1,2]

Program Cycle[3]

Read Data
from
NVM

Data Correct? — No → Report Programming Failure

Yes

All Locations Done? — No → Increment PC Address to Next Row

Yes

Done

Note 1: This step is optional if the device has already been erased or has not been previously programmed.
2: If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 3-22.
3: See Figure 3-19 or Figure 3-20.

FIGURE 3-19: **ONE-WORD PROGRAM CYCLE**

Program Cycle
(for Programming Data EEPROM, User ID and Configuration Words)

Load Data
for
NVM Command

Begin
Programming
Command
(Internally Timed)

Wait T_{PINT}
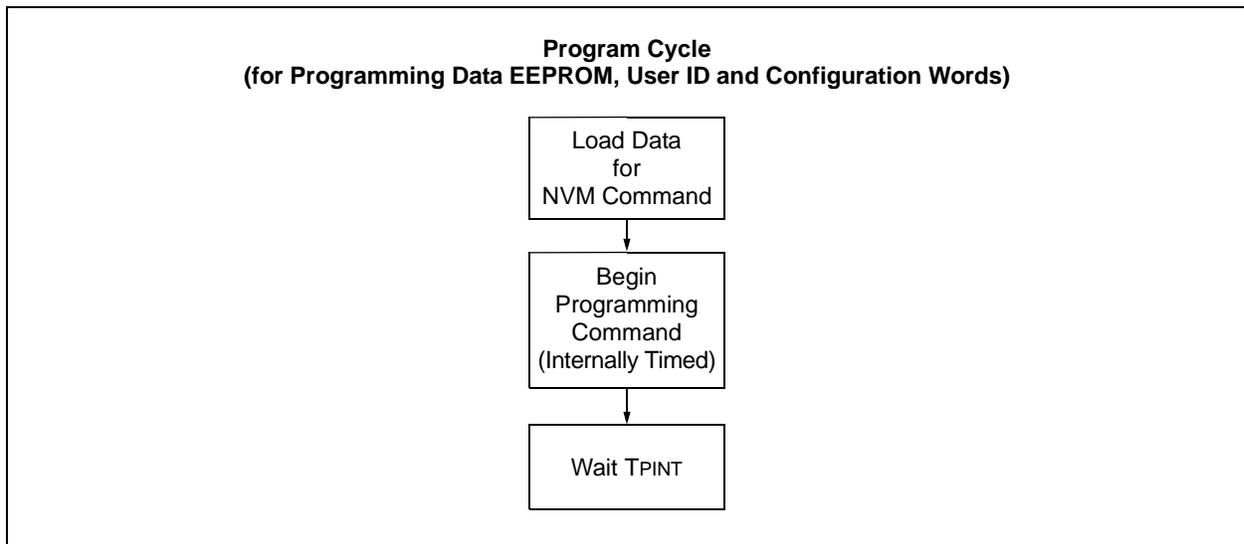
FIGURE 3-20: MULTIPLE WORD PROGRAM CYCLE

Program Cycle
(for Writing to Program Flash Memory)

Load Data for NVM — Latch 1

Increment Address

Load Data for NVM — Latch 2

●
●
●

Increment Address

Load Data for NVM — Latch n[1]

Begin Programming Command (Internally Timed)

Begin Programming Command (Externally Timed)

Wait T_{PINT}

Wait T_{PEXT}

End Externally Timed Programming Command

Wait T_{DIS}

Note 1: Refer to Table 3-3 for latch size.

FIGURE 3-21: **USER ID AND CONFIGURATION MEMORY PROGRAM FLOWCHART**

Note 1: This step is optional if the device is erased or not previously programmed.
2: See Figure 3-19.
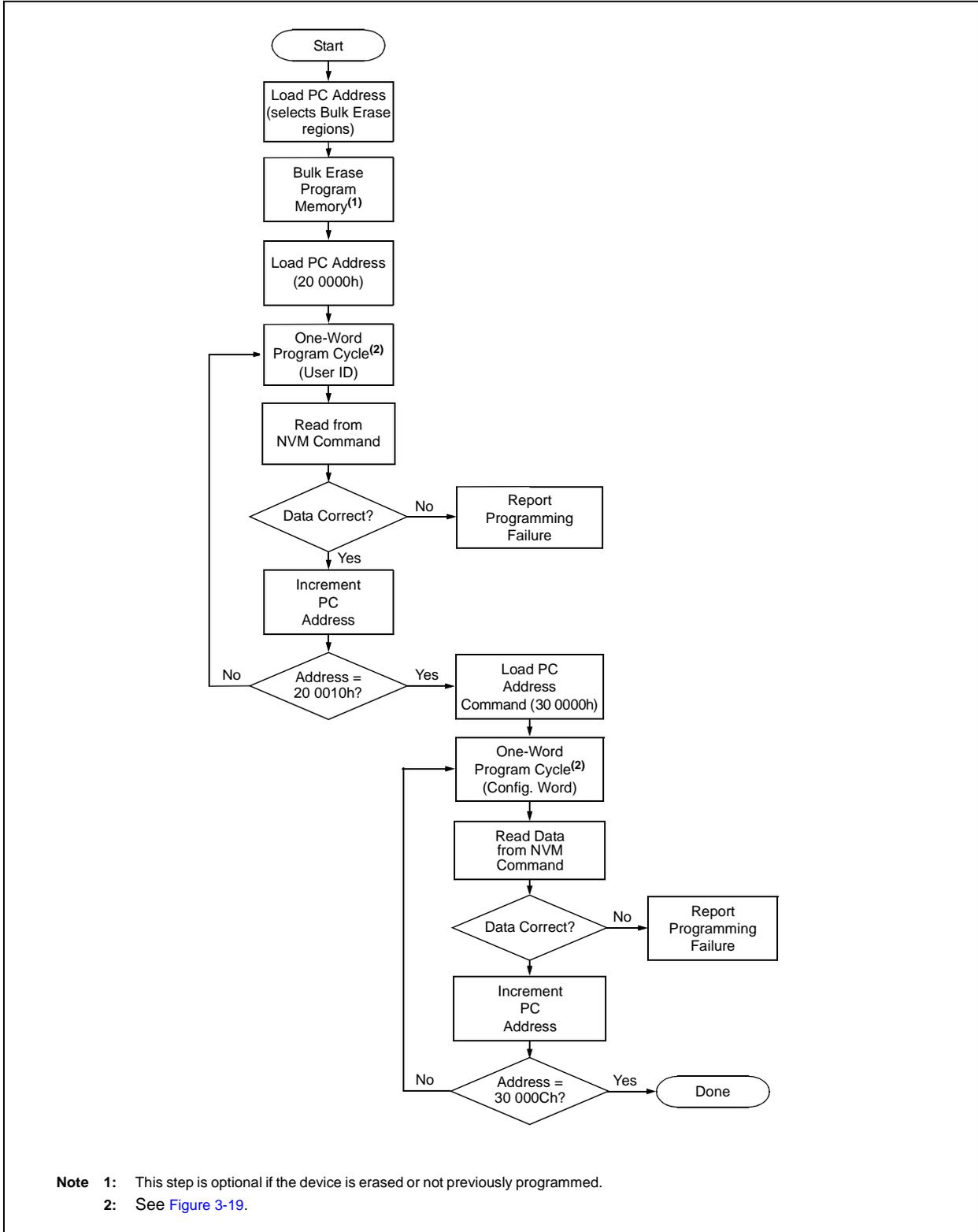
FIGURE 3-22: **BULK ERASE FLOWCHART**
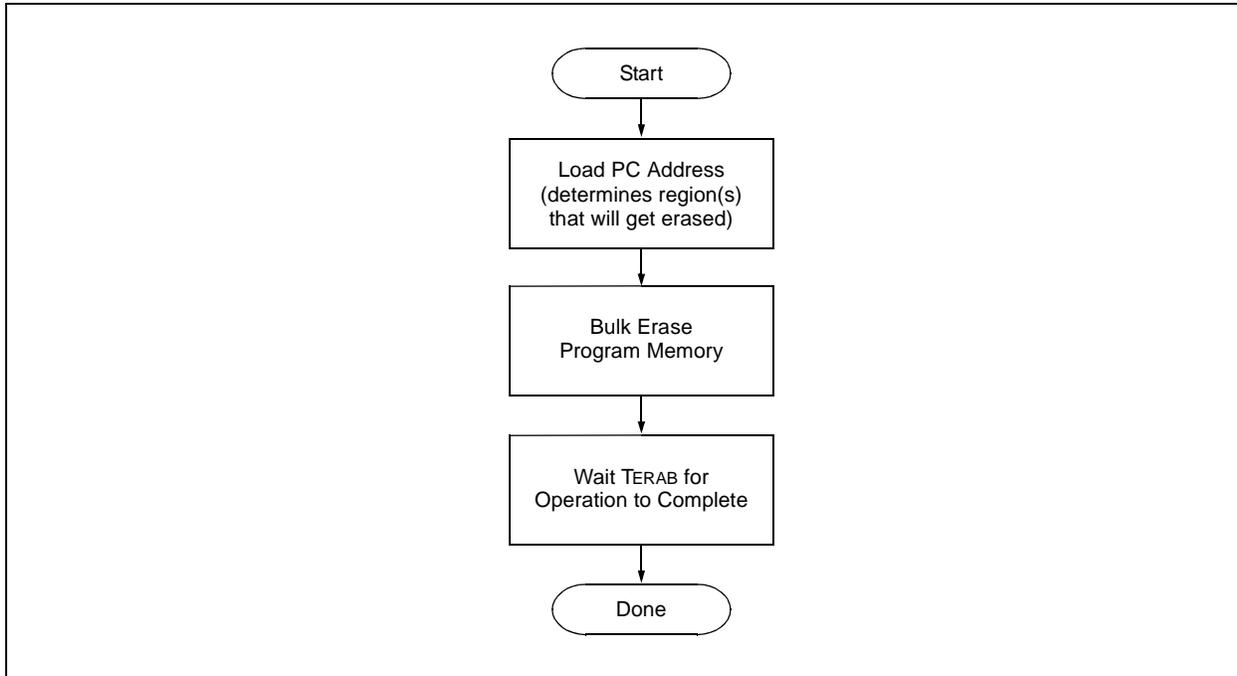
3.3 Code Protection

Code protection is controlled using the $\overline{\text{CP}}$ bit. When code protection is enabled, all program memory locations read as '0'. Further programming is disabled for the program memory until the next Bulk Erase operation is performed. Program memory can still be programmed and read during program execution.

The User ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

3.3.1 PROGRAM MEMORY

Code protection is enabled by programming the $\overline{\text{CP}}$ bit to '0'. The only way to disable code protection is to use the Bulk Erase Memory command (with the PC set to an address so as to Bulk Erase all program Flash contents).

3.3.2 DATA EEPROM MEMORY

Data EEPROM Memory protection is enabled by programming the $\overline{\text{CPD}}$ bit to '0'. The only way to disable code protection is to use the Bulk Erase Memory command.

3.4 Hex File Usage

3.4.1 EMBEDDING CONFIGURATION WORD INFORMATION IN THE HEX FILE

To allow portability of code, a programmer is required to read the Configuration Word locations from the Hex file. If Configuration Word information is not present in the Hex file, then a simple warning message should be issued. Similarly, while saving a Hex file, all Configuration Word information must be included. An option to not include the Configuration Word information may be provided. When embedding Configuration Word information in the Hex file, it should start at address, 300000h.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

3.4.2 EMBEDDING DATA EEPROM INFORMATION IN THE HEX FILE

To allow portability of code, a programmer is required to read the data EEPROM information from the Hex file. If data EEPROM information is not present, a simple warning message should be issued. Similarly, when saving a Hex file, all data EEPROM information must be included. An option to not include the data EEPROM information may be provided. When embedding data EEPROM information in the Hex file, it should start at address, F00000h.

Microchip Technology Inc. believes that this feature is important for the benefit of the end customer.

3.5 Checksum Computation

The checksum is calculated by two different methods, dependent on the setting of the $\overline{CP}$ Configuration bit. Refer to **Appendix B** for checksum computation examples.

3.5.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data, starting at address, 00 0000h, up to the maximum user-addressable location (e.g., 01 FFFFh for the PIC18(L)F67K40 device). Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

3.5.2 PROGRAM CODE PROTECTION ENABLED

When the MPLAB® IDE check box for "Configure → ID Memory... → Use Unprotected Checksum" is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the User ID. The unprotected checksum is distributed one nibble per ID location. Each nibble is right justified.

The checksum of a code-protected device is computed in the following manner:

- All of the User ID locations are added to create the sum ID
- The sum ID is then added to the Configuration bits
- All unimplemented Configuration bits are masked to '0'

| Note: | The checksum calculation differs depending on the code-protect setting. Since the code memory locations read out differently, depending on the code-protect setting, the examples in **Appendix B** describe how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Word and ID locations can always be read. |

PIC18(L)F6XK40

3.6 Electrical Specifications

Refer to the device-specific data sheet for absolute maximum ratings.

TABLE 3-4: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS			Standard Operating Conditions Production tested at +25°C				
Sym.	Characteristics		Min.	Typ.	Max.	Units	Conditions/Comments
	Programming Supply Voltages and Currents						
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	PICXXLFXXKXX	1.80	—	3.60	V	**Note 1**
		PICXXFXXKXX	2.30	—	5.50	V	
V_{PEW}	Read/Write and Row Erase Operations		V_{DDMIN}	—	V_{DDMAX}	V	
V_{BE}	Bulk Erase Operations		V_{BORMAX}	—	V_{DDMAX}	V	**Note 2**
I_{DDI}	Current on V_{DD}, Idle		—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming		—	—	5.0	mA	
	VPP						
I_{PP}	Current on $\overline{MCLR}$/VPP		—	—	600	µA	
V_{IHH}	High Voltage on $\overline{MCLR}$/VPP for Program/Verify Mode Entry		7.9	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ Rise Time (V_{IL} to V_{IHH}) for Program/Verify Mode Entry		—	—	1.0	µs	
	I/O Pins						
V_{IH}	(ICSPCLK, ICSPDAT, $\overline{MCLR}$/VPP) Input High Level		0.8 V_{DD}	—	V_{DD}	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}$/VPP) Input Low Level		V_{SS}	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT Output High Level		V_{DD} – 0.7 V_{DD} – 0.7 V_{DD} – 0.7	—	—	V	I_{OH} = 3.5 mA, V_{DD} = 5V I_{OH} = 3 mA, V_{DD} = 3.3V I_{OH} = 1 mA, V_{DD} = 1.8V
V_{OL}	ICSPDAT Output Low Level		—	—	V_{SS} + 0.6 V_{SS} + 0.6 V_{SS} + 0.6	V	I_{OL} = 8 mA, V_{DD} = 5V I_{OL} = 6 mA, V_{DD} = 3.3V I_{OL} = 1.8 mA, V_{DD} = 1.8V
	Programming Mode Entry and Exit						
T_{ENTS}	Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time before V_{DD} or $\overline{MCLR}\uparrow$		100	—	—	ns	
T_{ENTH}	Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time after V_{DD} or $\overline{MCLR}\uparrow$		250	—	—	µs	
	Serial Program/Verify						
T_{CKL}	Clock Low Pulse Width		100	—	—	ns	
T_{CKH}	Clock High Pulse Width		100	—	—	ns	
T_{DS}	Data in Setup Time before Clock$\downarrow$		100	—	—	ns	
T_{DH}	Data in Hold Time after Clock$\downarrow$		100	—	—	ns	
T_{CO}	Clock$\uparrow$ to Data Out Valid (during a Read Data command)		0	—	80	ns	

Note 1: Bulk Erased devices default to Brown-out Reset enabled with BORV = 1 (low trip point). V_{DDMIN} is the V_{BOR} threshold (with BORV = 1) when performing Low-Voltage Programming on a Bulk Erased device to ensure that the device is not held in Brown-out Reset.

2: The hardware requires V_{DD} to be above the BOR threshold, at the ~2.4V nominal setting, in order to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit settings. The threshold is the same for both F and LF devices, even though the LF devices may not have a user-configurable ~2.4V nominal BOR trip point setting. Refer to the microcontroller device data sheet specifications for min./typ./max. limits of the V_{BOR} level (at the BORV = 0 setting of F devices).

3: Externally timed writes are not supported for Configuration and Calibration bits.

TABLE 3-4: **AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE (CONTINUED)**

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at +25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
TLZD	Clock↓ to Data Low-Impedance (during a Read Data command)	0	—	80	ns	
THZD	Clock↓ to Data High-Impedance (during a Read Data command)	0	—	80	ns	
TDLY	Data Input not driven to Next Clock Input (delay required between command/data or command/command)	1.0	—	—	µs	
TERAB	Bulk Erase Cycle Time	—	—	25.2	ms	
TERAR	Row Erase Cycle Time	—	—	2.8	ms	
TPINT	Internally Timed Programming Operation Time	—	—	2.8	ms	Program memory
		—	—	5.6	ms	Configuration Words/ Data EEPROM Memory
TPEXT	Delay required between Begin Externally Timed Programming and End Externally Timed Programming Commands	1.0	—	2.1	ms	**Note 3**
TDIS	Delay required after End Externally Timed Programming Command	300	—	—	µs	
TEXIT	Time Delay when exiting Program/Verify Mode	1	—	—	µs	

Note 1: Bulk Erased devices default to Brown-out Reset enabled with BORV = 1 (low trip point). V$_{DDMIN}$ is the V$_{BOR}$ threshold (with BORV = 1) when performing Low-Voltage Programming on a Bulk Erased device to ensure that the device is not held in Brown-out Reset.

2: The hardware requires V$_{DD}$ to be above the BOR threshold, at the ~2.4V nominal setting, in order to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit settings. The threshold is the same for both F and LF devices, even though the LF devices may not have a user-configurable ~2.4V nominal BOR trip point setting. Refer to the microcontroller device data sheet specifications for min./typ./max. limits of the V$_{BOR}$ level (at the BORV = 0 setting of F devices).

3: Externally timed writes are not supported for Configuration and Calibration bits.

APPENDIX A: REVISION HISTORY

Revision A (11/2015)

Initial release of the document.

APPENDIX B: PIC18(L)F6XK40 DEVICE ID, CHECKSUMS AND PINOUT DESCRIPTIONS

TABLE B-1: CONFIGURATION WORD AND MASK

Device	Device ID	Config. 1L		Config. 1H		Config. 2L		Config. 2H		Config. 3L		Config. 3H		Config. 4L		Config. 4H		Config. 5L			Config. 5H			Config. 6L		Config. 6H	
		Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Unprotected	Code-Protected	Mask (Hex)	Unprotected	Code-Protected	Mask (Hex)	Word	Mask (Hex)	Word	Mask (Hex)
PIC18F67K40	6AC0h	FF	77	FF	29	FF	E3	FF	BF	FF	7F	FF	3F	FF	FF	FF	37	FF	FE	03	FF	FF	00	FF	FF	FF	02
PIC18F66K40	6AE0h	FF	77	FF	29	FF	E3	FF	BF	FF	7F	FF	3F	FF	0F	FF	37	FF	FE	03	FF	FF	00	FF	0F	FF	02
PIC18F65K40	6800h	FF	77	FF	29	FF	E3	FF	BF	FF	7F	FF	3F	FF	0F	FF	37	FF	FE	03	FF	FF	00	FF	0F	FF	02
PIC18LF67K40	6B20h	FF	77	FF	29	FF	E3	FF	BF	FF	7F	FF	3F	FF	FF	FF	37	FF	FE	03	FF	FF	00	FF	FF	FF	02
PIC18LF66K40	6B40h	FF	77	FF	29	FF	E3	FF	BF	FF	7F	FF	3F	FF	0F	FF	37	FF	FE	03	FF	FF	00	FF	0F	FF	02
PIC18LF65K40	6B60h	FF	77	FF	29	FF	E3	FF	BF	FF	7F	FF	3F	FF	0F	FF	37	FF	FE	03	FF	FF	00	FF	0F	FF	02

PIC18(L)F6XK40

TABLE B-2: CHECKSUM VALUES

Device	Checksum			
	Unprotected		Code-Protected	
	Blank	0AAh at First and Last Address	Blank	00AAh at First and Last Address
PIC18F67K40	053A	0490	054B	0546
PIC18F66K40	035A	02B0	036B	0366
PIC18F65K40	835A	82B0	0373	036E
PIC18(L)F67K40	053A	0490	054B	0546
PIC18(L)F66K40	035A	02B0	036B	0366
PIC18(L)F65K40	835A	82B0	0373	036E

EXAMPLE B-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED: PIC18(L)F65K40, BLANK DEVICE

PIC18(L)F65K40	Sum of Memory Addresses from 0000h to 7FFFh 8000h (8000h * 00FFh)

Configuration Word 1L ....FFh

Configuration Word 1L Mask 77h

Configuration Word 1H .... FFh

Configuration Word 1H Mask 29h

Configuration Word 2L .... FFh

Configuration Word 2L Mask E3h

Configuration Word 2H .... FFh

Configuration Word 2H Mask .... BFh

Configuration Word 3L .... FFh

Configuration Word 3L Mask 7Fh

Configuration Word 3H... FFh

Configuration Word 3H Mask 3Fh

Configuration Word 4L 0Fh

Configuration Word 4L Mask .... FFh

Configuration Word 4H .... FFh

Configuration Word 4H Mask 37h

Configuration Word 5L Unprotected .... FFh

Configuration Word 5L Mask 03h

Configuration Word 5H Unprotected .... FFh

Configuration Word 5H Mask 00h

Configuration Word 6L .... FFh

Configuration Word 6L Mask 0Fh

Configuration Word 6H .... FFh

Configuration Word 6H Mask 02h

Checksum = C000h + (FFh AND 77h) + (FFh AND 29h) + (FFh AND E3h) + (FFh AND BFh)
+ (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 0Fh) + (FFh AND 37h)
+ (FFh AND 03h) + (FFh AND 00h) + (FFh AND 0Fh) + (FFh AND 02h)
= C000h + 77h + 29h + E3h + BFh + 7Fh + 3Fh + 0Fh + 37h + 03h + 00h + 0Fh + 02h
= 835Ah

PIC18(L)F6XK40

EXAMPLE B-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED: PIC18(L)F65K40, 00AAh AT FIRST AND LAST ADDRESS

PIC18(L)F65K40		
	Sum of Memory Addresses from 0000h to 7FFFh	7F56h (AAh + (7FFEh * 00FFh) + AAh)
	Configuration Word 1L ....FFh	
	Configuration Word 1L Mask 77h	
	Configuration Word 1H ....FFh	
	Configuration Word 1H Mask 29h	
	Configuration Word 2L ....FFh	
	Configuration Word 2L Mask E3h	
	Configuration Word 2H ....FFh	
	Configuration Word 2H Mask ....BFh	
	Configuration Word 3L ....FFh	
	Configuration Word 3L Mask 7Fh	
	Configuration Word 3H ....FFh	
	Configuration Word 3H Mask 3Fh	
	Configuration Word 4L ....FFh	
	Configuration Word 4L Mask 0Fh	
	Configuration Word 4H ....FFh	
	Configuration Word 4H Mask 37h	
	Configuration Word 5L Unprotected ....FFh	
	Configuration Word 5L Mask 03h	
	Configuration Word 5H Unprotected ....FFh	
	Configuration Word 5H Mask 00h	
	Configuration Word 6L ....FFh	
	Configuration Word 6L Mask 0Fh	
	Configuration Word 6H ....FFh	
	Configuration Word 6H Mask 02h	

Checksum = BF56h + (FFh AND 77h) + (FFh AND 29h) + (FFh AND E3h) + (FFh AND BFh)

+ (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 0Fh) + (FFh AND 37h)

+ (FFh AND 03h) + (FFh AND 00h) + (FFh AND 0Fh) + (FFh AND 02h)

= BF56h + 77h + 29h + E3h + BFh + 7Fh + 3Fh + 0Fh + 37h + 03h + 00h + 0Fh + 02h

= 82B0h

EXAMPLE B-3:   CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED: PIC18(L)F65K40, BLANK DEVICE

PIC18(L)F65K40	Configuration Word 1L ....FFh
	Configuration Word 1L Mask 77h
	Configuration Word 1H ....FFh
	Configuration Word 1H Mask 29h
	Configuration Word 2L ....FFh
	Configuration Word 2L Mask E3h
	Configuration Word 2H ....FFh
	Configuration Word 2H Mask ....BFh
	Configuration Word 3L ....FFh
	Configuration Word 3L Mask 7Fh
	Configuration Word 3H..FFh
	Configuration Word 3H Mask 3Fh
	Configuration Word 4L ....FFh
	Configuration Word 4L Mask 0Fh
	Configuration Word 4H ....FFh
	Configuration Word 4H Mask 37h
	Configuration Word 5L Protected ....FEh
	Configuration Word 5L Mask 03h
	Configuration Word 5H Protected ....FFh
	Configuration Word 5H Mask 00h
	Configuration Word 6L ....FFh
	Configuration Word 6L Mask 0Fh
	Configuration Word 6H ....FFh
	Configuration Word 6H Mask 02h

Checksum = (FFh AND 77h) + (FFh AND 29h) + (FFh AND E3h) + (FFh AND BFh)

   + (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 0Fh) + (FFh AND 37h)

   + (FEh AND 03h) + (FFh AND 00h) + (FFh AND 0Fh) + (FFh AND 02h) + SUM_ID

= 77h + 29h + E3h + BFh + 7Fh + 3Fh + 0Fh + 37h + 02h + 00h + 0Fh + 02h + 001Ah

= 0373h

SUM_ID = Bytewise sum of lower four bits of all User ID locations

SUM_ID = 0008h + 0003h + 0005h + 000Ah + 0000h + 0000h + 0000h + 0000h = 001Ah

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EXAMPLE B-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED: PIC18(L)F65K40, 00AAh AT FIRST AND LAST ADDRESS

PIC18(L)F65K40	Configuration Word 1L ....FFh
	Configuration Word 1L Mask 77h
	Configuration Word 1H ....FFh
	Configuration Word 1H Mask 29h
	Configuration Word 2L ....FFh
	Configuration Word 2L Mask E3h
	Configuration Word 2H ....FFh
	Configuration Word 2H Mask ....BFh
	Configuration Word 3L ....FFh
	Configuration Word 3L Mask 7Fh
	Configuration Word 3H...FFh
	Configuration Word 3H Mask 3Fh
	Configuration Word 4L ....FFh
	Configuration Word 4L Mask 0Fh
	Configuration Word 4H ....FFh
	Configuration Word 4H Mask 37h
	Configuration Word 5L Protected ....FEh
	Configuration Word 5L Mask 03h
	Configuration Word 5H Protected ....FFh
	Configuration Word 5H Mask 00h
	Configuration Word 6L Protected ....FFh
	Configuration Word 6L Mask 0Fh
	Configuration Word 6H Protected ....FFh
	Configuration Word 6H Mask 02h
	Checksum = (FFh AND 77h) + (FFh AND 29h) + (FFh AND E3h) + (FFh AND BFh)
	$\quad\quad$ + (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 03h) + (FFh AND 37h)
	$\quad\quad$ + (FEh AND 03h) + (FFh AND 00h) + (FFh AND 03h) + (FFh AND 02h) + SUM_ID
	$\quad$ = 77h + 29h + E3h + BFh + 7Fh + 3Fh + 0Fh + 37h + 02h + 00h + 0Fh + 02h + 0015h
	$\quad$ = 036Eh
SUM_ID = Bytewise sum of lower four bits of all User ID locations	
SUM_ID = 0008h + 0002h + 000Bh + 0000h + 0000h + 0000h + 0000h + 0000h = 0015h	

TABLE B-3: **PROGRAMMING PIN LOCATIONS BY PACKAGE TYPE**

Device	Package	Package Code	Package Drawing Number[1]	V$_{DD}$ PIN	V$_{SS}$ PIN	$\overline{MCLR}$ PIN	$\overline{MCLR}$ PORT	ICSPCLK PIN	ICSPCLK PORT	ICSPDAT PIN	ICSPDAT PORT
PIC18(L)F65K40	64-pin TQFP	PT	C04-085	10,38	9,41	7	RG5	42	RB6	37	RB7
	64-pin QFN	MR	C04-149	10,38	9,41	7	RG5	42	RB6	37	RB7
PIC18(L)F66K40	64-pin TQFP	PT	C04-085	10,38	9,41	7	RG5	42	RB6	37	RB7
	64-pin QFN	MR	C04-149	10,38	9,41	7	RG5	42	RB6	37	RB7
PIC18(L)F67K40	64-pin TQFP	PT	C04-085	10,38	9,41	7	RG5	42	RB6	37	RB7
	64-pin QFN	MR	C04-149	10,38	9,41	7	RG5	42	RB6	37	RB7

Note 1: The most current package drawings can be found in the Microchip Packaging Specification, DS00000049, found at http://www.microchip.com/packaging. The drawing numbers listed above do not include the current revision designator which is added at the end of the number.

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TABLE B-4: **SUMMARY OF CONFIGURATION WORDS**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
30 0000h	CONFIG 1L	—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0	1111 1111
30 0001h	CONFIG 1H	—	—	FCMEN	—	CSWEN	—	—	CLKOUTEN	1111 1111
30 0002h	CONFIG 2L	BOREN1	BOREN0	LPBOREN	—	—	—	PWRTE	MCLRE	1111 1111
30 0003h	CONFIG 2H	XINST	—	DEBUG	STVREN	PPS1WAY	ZCDDIS	BORV1	BORV0	1111 1111
30 0004h	CONFIG 3L	—	WDTE1	WDTE0	WDTCPS4	WDTCPS3	WDTCPS2	WDTCPS1	WDTCPS0	1111 1111
30 0005h	CONFIG 3H	—	—	WDTCCS2	WDTCCS1	WDTCCS0	WDTCWS2	WDTCWS1	WDTCWS0	1111 1111
30 0006h	CONFIG 4L	WRT7	WRT6	WRT5	WRT4	WRT3	WRT2	WRT1	WRT0	1111 1111
30 0007h	CONFIG 4H	—	—	LVP	SCANE	—	WRTD	WRTB	WRTC	1111 1111
30 0008h	CONFIG 5L	—	—	—	—	—	—	CPD	CP	1111 1111
30 000Ah	CONFIG 6L	EBTR7	EBTR6	EBTR5	EBTR4	EBTR3	EBTR2	EBTR1	EBTR0	1111 1111
30 000Bh	CONFIG 6H	—	—	—	—	—	—	EBTRB	—	1111 1111

REGISTER B-1: **CONFIGURATION WORD 1L (30 0000h) – OSCILLATORS**

U-1	R/W-1	R/W-1	R/W-1	U-1	R/W-1	R/W-1	R/W-1
—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **Unimplemented:** Read as '1'

bit 6-4   **RSTOSC<2:0>:** Power-up Default Value for COSC bits

This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

111 = EXTOSC operating per FEXTOSC<2:0> bits (device manufacturing default)
110 = HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1
101 = LFINTOSC
100 = SOSC
011 = Reserved
010 = EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC<2:0> bits
001 = Reserved
000 = HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1; resets COSC/NOSC to 3'b110

bit 3   **Unimplemented:** Read as '1'

bit 2-0   **FEXTOSC<2:0>:** FEXTOSC External Oscillator Mode Selection bits

111 = EC (External Clock) above 8 MHz; PFM set to high power (device manufacturing default)
110 = EC (External Clock) for 500 kHz to 8 MHz; PFM set to medium power
101 = EC (External Clock) below 500 kHz; PFM set to low power
100 = Oscillator is not enabled
011 = Reserved (do not use)
010 = HS (crystal oscillator) above 8 MHz; PFM set to high power
001 = XT (crystal oscillator) above 500 kHz, below 8 MHz; PFM set to medium power
000 = LP (crystal oscillator) optimized for 32.768 kHz; PFM set to low power

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REGISTER B-2: **CONFIGURATION WORD 1H (30 0001h) – OSCILLATORS**

U-1	U-1	R/W-1	U-1	R/W-1	U-1	U-1	R/W-1
—	—	FCMEN	—	CSWEN	—	—	CLKOUTEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '1'

bit 5   **FCMEN:** Fail-Safe Clock Monitor Enable bit
                      1 = FSCM timer is enabled
                      0 = FSCM timer is disabled

bit 4   **Unimplemented:** Read as '1'

bit 3   **CSWEN:** Clock Switch Enable bit
                      1 = Writing to NOSC and NDIV is allowed
                      0 = The NOSC and NDIV bits cannot be changed by user software

bit 2-1   **Unimplemented:** Read as '1'

bit 0   **CLKOUTEN:** Clock Out Enable bit
                      If FEXTOSC<2:0> = EC (high, mid or low) or Not Enabled:
                      1 = CLKOUT function is disabled; I/O or oscillator function on OSC2
                      0 = CLKOUT function is enabled; F$_{OSC}$/4 clock appears at OSC2
                      Otherwise:
                      This bit is ignored.

REGISTER B-3: **CONFIGURATION WORD 2L (30 0002h) – SUPERVISOR**

R/W-1	R/W-1	R/W-1	U-1	U-1	U-1	R/W-1	R/W-1
BOREN1	BOREN0	LPBOREN	—	—	—	PWRTE	MCLRE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6 **BOREN<1:0>:** Brown-out Reset Enable bits

When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit.
11 = Brown-out Reset is enabled, SBOREN bit is ignored
10 = Brown-out Reset is enabled while running, disabled in Sleep; SBOREN is ignored
01 = Brown-out Reset is enabled according to SBOREN
00 = Brown-out Reset is disabled

bit 5 **LPBOREN:** Low-Power BOR Enable bit

1 = ULPBOR is disabled
0 = ULPBOR is enabled

bit 4-2 **Unimplemented:** Read as '1'

bit 1 **PWRTE:** Power-up Timer Enable bit

1 = PWRT is disabled
0 = PWRT is enabled

bit 0 **MCLRE:** Master Clear (MCLR) Enable bit

If LVP = 1:
RE3 pin function is MCLR.

If LVP = 0:
1 = MCLR pin is MCLR
0 = MCLR pin function is a port defined function

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R/W-1	U-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{XINST}}$	—	$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	ZCDDIS	BORV1[1]	BORV0[1]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **XINST:** Extended Instruction Set Enable bit

1 = Extended instruction set and Indexed Addressing mode are disabled (Legacy mode)
0 = Extended instruction set and Indexed Addressing mode are enabled

bit 6   **Unimplemented:** Read as '1'

bit 5   **DEBUG:** Debugger Enable bit

1 = Background debugger is disabled
0 = Background debugger is enabled

bit 4   **STVREN:** Stack Overflow/Underflow Reset Enable bit

1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 3   **PPS1WAY:** PPSLOCK One-Way Set Enable bit

1 = PPSLOCK bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
0 = PPSLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

bit 2   **ZCDDIS:** ZCD Disable bit

1 = ZCD is disabled; ZCD can be enabled by setting the ZCDSEN bit of the ZCDCON register
0 = ZCD is always enabled

bit 1-0   **BORV<1:0>:** Brown-out Reset Voltage Selection bits[1]

PIC18FXXK40 Devices:
11 = Brown-out Reset Voltage (V$_{BOR}$) is set to 2.45V
10 = Brown-out Reset Voltage (V$_{BOR}$) is set to 2.45V
01 = Brown-out Reset Voltage (V$_{BOR}$) is set to 2.7V
00 = Brown-out Reset Voltage (V$_{BOR}$) is set to 2.85V
PIC18LFXXK40 Device:
11 = Brown-out Reset Voltage (V$_{BOR}$) is set to 1.90V
10 = Brown-out Reset Voltage (V$_{BOR}$) is set to 2.45V
01 = Brown-out Reset Voltage (V$_{BOR}$) is set to 2.7V
00 = Brown-out Reset Voltage (V$_{BOR}$) is set to 2.85V

Note 1:   The higher voltage setting is recommended for operation at or above 16 MHz.

REGISTER B-5: **CONFIGURATION WORD 3L (30 0004h) – WINDOWED WATCHDOG TIMER**

U-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	WDTE1	WDTE0	WDTCPS4	WDTCPS3	WDTCPS2	WDTCPS1	WDTCPS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7   **Unimplemented:** Read as '1'

bit 6-5   **WDTE<1:0>:** WDT Operating Mode bits

         11 = WDT is enabled regardless of Sleep; SWDTEN is ignored
         10 = WDT is enabled while Sleep = 0, suspended when Sleep = 1; SWDTEN is ignored
         01 = WDT is enabled/disabled by the SWDTEN bit in WDTCON0
         00 = WDT is disabled, SWDTEN is ignored

bit 4-0   **WDTCPS<4:0>:** WDT Period Select bits

WDTCPS<4:0>	WDTPS at POR			Software Control of WDTPS?
	Value	Divider Ratio		
			Typical Time-out (F_{IN} = 31 kHz)	
11111	01011	1:65536	2^{16}	2s	Yes
10011 ... 11110	10011 ... 11110	1:32	2^5	1 ms	No
10010	10010	1:8388608	2^{23}	256s	No
10001	10001	1:4194304	2^{22}	128s	
10000	10000	1:2097152	2^{21}	64s	
01111	01111	1:1048576	2^{20}	32s	
01110	01110	1:524299	2^{19}	16s	
01101	01101	1:262144	2^{18}	8s	
01100	01100	1:131072	2^{17}	4s	
01011	01011	1:65536	2^{16}	2s	
01010	01010	1:32768	2^{15}	1s	
01001	01001	1:16384	2^{14}	512 ms	
01000	01000	1:8192	2^{13}	256 ms	
00111	00111	1:4096	2^{12}	128 ms	
00110	00110	1:2048	2^{11}	64 ms	
00101	00101	1:1024	2^{10}	32 ms	
00100	00100	1:512	2^9	16 ms	
00011	00011	1:256	2^8	8 ms	
00010	00010	1:128	2^7	4 ms	
00001	00001	1:64	2^6	2 ms	
00000	00000	1:32	2^5	1 ms	

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REGISTER B-6:   CONFIGURATION WORD 3H (30 0005h) – WINDOWED WATCHDOG TIMER

U-1	U-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WDTCCS2	WDTCCS1	WDTCCS0	WDTCWS2	WDTCWS1	WDTCWS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '1'

bit 5-3   **WDTCCS<2:0>:** WDT Input Clock Selector bits

If WDTE<1:0> Fuses = 2'b00:
This bit is ignored.

Otherwise:
111 = Software control
110 = Reserved (default to LFINTOSC)
•
•
•
010 = Reserved (default to LFINTOSC)
001 = WDT reference clock is the 31.25 kHz HFINTOSC (MFINTOSC)
000 = WDT reference clock is the 31.0 kHz LFINTOSC (default value)

bit 2-0   **WDTCWS<2:0>:** WDT Window Select bits

WDTCWS	Window at POR			Software Control of Window	Keyed Access Required?
	Value	Window Delay Percent of Time	Window Opening Percent of Time		
111	111	n/a	100	Yes	No
110	111	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

REGISTER B-7: CONFIGURATION WORD 4L (30 0006h) – MEMORY WRITE PROTECTION

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WRT7[1]	WRT6[1]	WRT5[1]	WRT4[1]	WRT3[1]	WRT2[1]	WRT1[1]	WRT0[1]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-0   **WRT*n*:** User NVM Self-Write Protection bits[1]
  1 = Memory Block *n* is NOT write-protected
  0 = Memory Block *n* is write-protected

Note 1: Refer to Table 2-2 for details on implementation of the individual WRTx bits.

REGISTER B-8: CONFIGURATION WORD 4H (30 0007h) – MEMORY WRITE PROTECTION

U-1	U-1	R/W-1	R/W-1	U-1	R/W-1	R/W-1	R/W-1
—	—	LVP	SCANE	—	WRTD	WRTB	WRTC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '1'

bit 5   **LVP:** Low-Voltage Programming Enable bit
  1 = Low-Voltage Programming is enabled; $\overline{MCLR}$/VPP pin function is $\overline{MCLR}$, MCLRE Configuration bit is ignored
  0 = HV on $\overline{MCLR}$/VPP must be used for programming
  The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode or accidentally eliminating LVP mode from the configuration state.

bit 4   **SCANE:** Scanner Enable bit
  1 = Scanner module is available for use, SCANMD bit enables the module
  0 = Scanner module is NOT available for use, SCANMD bit is ignored

bit 3   **Unimplemented:** Read as '1'

bit 2   **WRTD:** Data EEPROM Write Protection bit
  1 = Data EEPROM is NOT write-protected
  0 = Data EEPROM is write-protected

bit 1   **WRTB:** Boot Block Write Protection bit
  1 = Boot block is NOT write-protected
  0 = Boot block is write-protected

bit 0   **WRTC:** Configuration Register Write Protection bit
  1 = Configuration register is NOT write-protected
  0 = Configuration register is write-protected

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REGISTER B-9: **CONFIGURATION WORD 5L (30 0008h) – CODE PROTECTION**

U-1	U-1	U-1	U-1	U-1	U-1	R/W-1	R/W-1
—	—	—	—	—	—	$\overline{CPD}$	$\overline{CP}$

bit 7 — bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2　**Unimplemented:** Read as '1'

bit 1　$\overline{CPD}$**:** Data NVM Memory Code Protection bit
　1 = Data NVM code protection is disabled
　0 = Data NVM code protection is enabled

bit 0　$\overline{CP}$**:** User NVM Program Memory Code Protection bit
　1 = User NVM code protection is disabled
　0 = User NVM code protection is enabled

REGISTER B-10: **CONFIGURATION WORD 6L (30 000Ah) – MEMORY READ PROTECTION**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
EBTR7[1]	EBTR6[1]	EBTR5[1]	EBTR4[1]	EBTR3[1]	EBTR2[1]	EBTR1[1]	EBTR0[1]

bit 7 — bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0　**EBTR***n***:** Table Read Protection bits[1]
　1 = Memory Block *n* is NOT protected from table reads executed in other blocks
　0 = Memory Block *n* is protected from table reads executed in other blocks

Note 1: Refer to Table 2-2 for details on implementation of the individual EBTRx bits.

REGISTER B-11: **CONFIGURATION WORD 6H (30 000Bh) – MEMORY READ PROTECTION**

U-1	U-1	U-1	U-1	U-1	U-1	R/W-1	U-1
—	—	—	—	—	—	EBTRB	—

bit 7 — bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2　**Unimplemented:** Read as '1'

bit 1　**EBTRB:** Table Read Protection bit
　1 = Memory boot block is NOT protected from table reads executed in other blocks
　0 = Memory boot block is protected from table reads executed in other blocks

bit 0　**Unimplemented:** Read as '1'

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