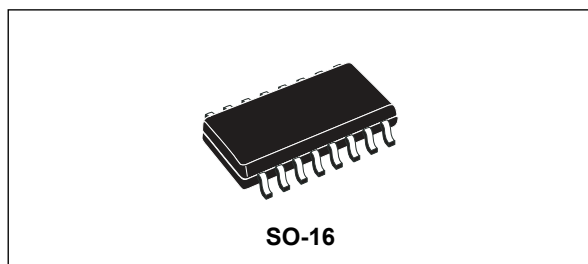


## Galvanically isolated 4 A half-bridge gate driver

Datasheet - production data



### Features

- 1700 V dual channel gate driver
- Driver current capability: 4 A sink / source at 25 °C
- $dV/dt$  transient immunity  $\pm 100$  V/ns
- Overall input-output propagation delay: 80 ns
- UVLO function
- Interlocking function
- Dedicated SD and BRAKE pins
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Standby function

### Applications

- Motor driver for industrial drives, factory automation, home appliances and fans.
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

### Description

The STGAP2D is a half-bridge gate driver which isolates the gate driving channels from the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for high power inverter applications such as motor drivers in industrial applications.

The device integrates protection functions: dedicated SD and BRAKE pins are available, UVLO and thermal shutdown are included to easily design high reliability systems, and the interlocking function prevents outputs from being high at the same time.

The input to output propagation delay results are contained within 80 ns, providing high PWM control accuracy.

A standby mode is available in order to reduce idle power consumption.

# Contents

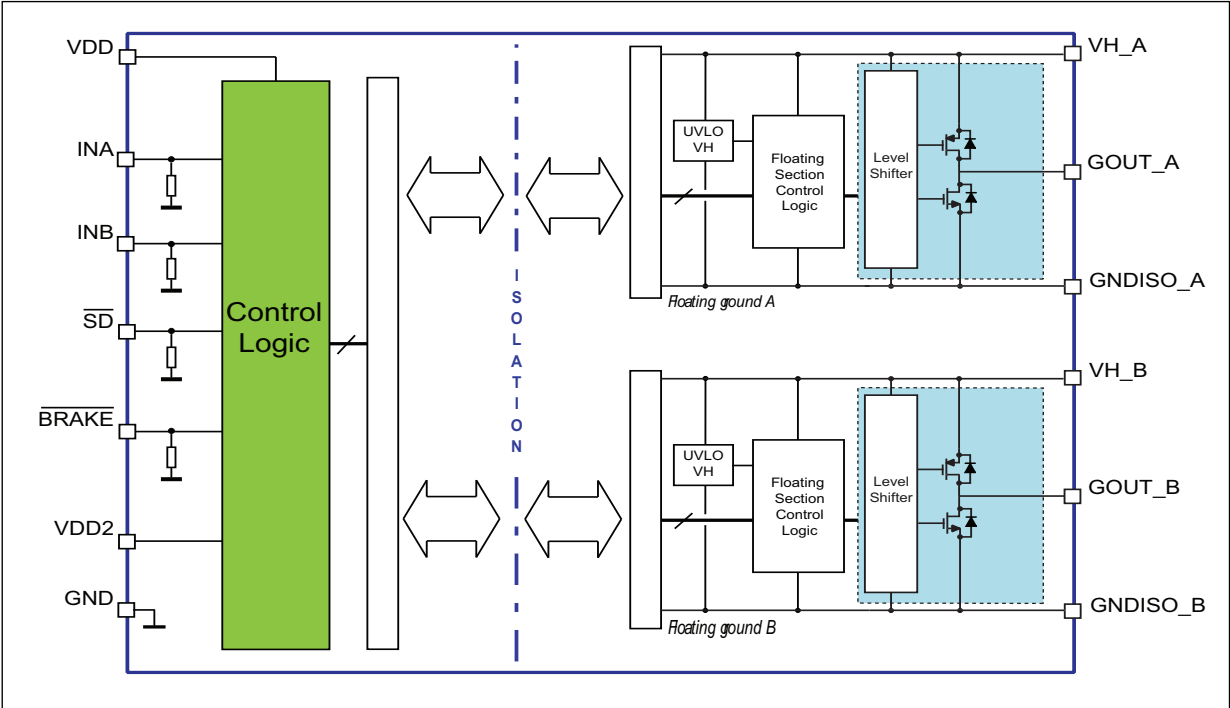
<b>1</b>	<b>Block diagram</b>	<b>4</b>
<b>2</b>	<b>Pin description and connection diagram</b>	<b>5</b>
<b>3</b>	<b>Electrical data</b>	<b>6</b>
3.1	Absolute maximum ratings	6
3.2	Thermal data	6
3.3	Recommended operating conditions	6
<b>4</b>	<b>Electrical characteristics</b>	<b>8</b>
4.1	Electrical characteristics	8
<b>5</b>	<b>Functional description</b>	<b>10</b>
5.1	Gate driving power supply and UVLO	10
5.2	Power-up, power-down and 'safe state'	10
5.3	Control inputs	11
5.4	Watchdog	11
5.5	Thermal shutdown protection	11
5.6	Standby function	11
<b>6</b>	<b>Typical application diagram</b>	<b>13</b>
<b>7</b>	<b>Layout</b>	<b>14</b>
7.1	Layout guidelines and considerations	14
7.2	Layout example	15
<b>8</b>	<b>Testing and characterization information</b>	<b>16</b>
<b>9</b>	<b>Package information</b>	<b>17</b>
<b>10</b>	<b>Suggested land pattern</b>	<b>19</b>
<b>11</b>	<b>Ordering information</b>	<b>20</b>

---

12	Revision history .....	20
----	------------------------	----

1 Block diagram

Figure 1. Block diagram



## 2 Pin description and connection diagram

Figure 2. Pin connection (top view)

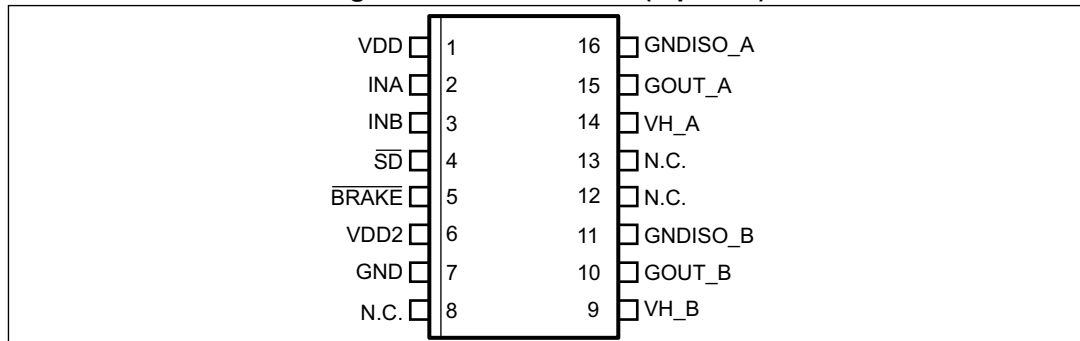


Table 1. Pin description

Pin #	Pin Name	Type	Function
1	VDD	Power supply	Control logic supply voltage.
2	INA	Logic input	Control logic input for Channel A, active high.
3	INB	Logic input	Control logic input for Channel B, active high.
4	$\overline{SD}$	Logic input	Shutdown input, active low.
5	$\overline{BRAKE}$	Logic input	Control logic input, active low.
6	VDD2	Power supply	Must be connected to VDD.
7	GND	Power supply	Control logic ground.
9	VH_B	Power supply	Channel B gate driving positive supply.
10	GOUT_B	Analog output	Channel B Sink/Source output.
11	GNDISO_B	Power supply	Channel B gate driving isolated ground.
14	VH_A	Power supply	Channel A gate driving positive supply.
15	GOUT_A	Analog output	Channel A Sink/Source output.
16	GNDISO_A	Power supply	Channel A gate driving isolated ground.
Others			Not connected.

### 3 Electrical data

#### 3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD, VDD2	Logic supply voltage vs. GND		-0.3	6.5	V
V <sub>LOGIC</sub>	Logic pins voltage vs. GND		-0.3	6.5	V
VH <sub>x</sub>	Positive supply voltage (VH <sub>x</sub> vs. GNDISO <sub>x</sub> )		-0.3	28	V
V <sub>OUT</sub>	Voltage on gate driver outputs (GOUT <sub>x</sub> vs. GNDISO <sub>x</sub> )		- 0.3	VH <sub>x</sub> + 0.3	V
V <sub>iso</sub>	Input to output isolation voltage (GND vs. GNDISO <sub>x</sub> )	DC or peak	-1700	+1700	V
T <sub>J</sub>	Junction temperature		-40	150	°C
T <sub>S</sub>	Storage temperature		-50	150	°C
P <sub>Din</sub>	Power Dissipation input chip	T <sub>A</sub> = 25 °C		10	mW
P <sub>Dout</sub>	Power Dissipation output chip	T <sub>A</sub> = 25 °C		1.16	W
ESD	HBM (human body model)		2		kV

#### 3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
R <sub>th(JA)</sub>	Thermal resistance junction to ambient	SO-16	90	°C/W

#### 3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD, VDD2	Logic supply voltage vs. GND	-	3	5.5	V
V <sub>LOGIC</sub>	Logic pins voltage vs. GND	-	0	5.5	V
VH <sub>x</sub>	Positive supply voltage (VH <sub>x</sub> vs. GNDISO <sub>x</sub> )	-		26	V
F <sub>SW</sub>	Maximum switching frequency <sup>(1)</sup>	-		1	MHz

Table 4. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
$T_{OUT}$	Pulse width	-	100		ns
$T_J$	Operating Junction Temperature	-	-40	125	°C

1. Actual limit depends on power dissipation and  $T_J$ .

## 4 Electrical characteristics

### 4.1 Electrical characteristics

Table 5. Electrical characteristics ( $T_J = 25\text{ }^{\circ}\text{C}$ ,  $VH\_x = 15\text{ V}$ ,  $VDD = 5\text{ V}$ , unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Dynamic characteristics</b>							
$t_{Don}$	INA, INB, SD, BRAKE	Input to output propagation delay ON		40	80	100	ns
$t_{Doff}$	INA, INB, SD, BRAKE	Input to output propagation delay OFF		40	80	100	ns
$t_r$		Rise time	$C_L = 4.7\text{ nF}$ , 10% ÷ 90%		30		ns
$t_f$		Fall time	$C_L = 4.7\text{ nF}$ , 10% ÷ 90%		30		ns
MT		Matching time <sup>(1)</sup>	DT = 5 V			20	ns
$t_{degitch}$	INA, INB, SD, BRAKE	Inputs deglitch filter			20	40	ns
CMTI <sup>(2)</sup>		Common-mode transient immunity, $ dV_{ISO}/dt $	$V_{CM} = 1500\text{ V}$ , see <a href="#">Figure 9</a>	100			V/ns
<b>Supply voltage</b>							
$VH_{on}$	-	$VH\_x$ UVLO turn-on threshold		8	9.1	10.5	V
$VH_{off}$	-	$VH\_x$ UVLO turn-off threshold		7	8.4	9.5	V
$VH_{hyst}$	-	$VH\_x$ UVLO hysteresis		0.5	0.9	1.4	V
$I_{QHU\_A}$ , $I_{QHU\_B}$	-	$VH\_x$ under-voltage quiescent supply current	$VH\_x = 4\text{ V}$		150	250	$\mu\text{A}$
$I_{QH\_A}$ , $I_{QH\_B}$	-	$VH\_x$ quiescent supply current			1.3	2.5	mA
$I_{QHSBY\_A}$ , $I_{QHSBY\_B}$	-	Standby $VH\_x$ quiescent supply current			400	600	$\mu\text{A}$
SafeClp	-	GOFF active clamp	$I_{GOFF} = 0.2\text{ A}$ ; $VH$ floating		2	2.5	V
$I_{QDD}$	-	VDD quiescent supply current			1	2	mA
$I_{QDDSBY}$	-	Standby VDD quiescent supply current	Standby mode		40	80	$\mu\text{A}$
<b>Logic inputs</b>							
$V_{il}$	INA, INB, SD, BRAKE	Low level logic threshold voltage		$0.29 \cdot VDD$	$1/3 \cdot VDD$	$0.37 \cdot VDD$	V



Table 5. Electrical characteristics ( $T_J = 25\text{ }^{\circ}\text{C}$ ,  $V_{H\_x} = 15\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{ih}$	INA, INB, SD, BRAKE	High level logic threshold voltage		$0.62 \cdot V_{DD}$	$2/3 \cdot V_{DD}$	$0.72 \cdot V_{DD}$	V
$I_{logic\_h}$	INA, INB, SD, BRAKE	Logic inputs high-level input bias current	$V_{logic} = 5\text{ V}$	33	50	77	$\mu\text{A}$
$I_{logic\_l}$	INA, INB, SD, BRAKE	Logic inputs low-level input bias current	$V_{logic} = 0\text{ V}$			1	$\mu\text{A}$
$R_{pd}$	INA, INB, SD, BRAKE	Logic inputs pull-down resistor		65	100	150	$\text{k}\Omega$
<b>Driver buffer section</b>							
$I_{GON}$	-	Source short-circuit current	$T_J = 25\text{ }^{\circ}\text{C}$		4		A
			$T_J = -40 \div +125\text{ }^{\circ}\text{C}^{(2)}$	3		5	
$I_{GOFF}$	-	Sink short-circuit current	$T_J = 25\text{ }^{\circ}\text{C}$		4		A
			$T_J = -40 \div +125\text{ }^{\circ}\text{C}^{(2)}$	3		5	
$V_{GONH}$	-	$G_{ON}$ output high level voltage	$I_{GON} = 100\text{ mA}$	$V_{H\_x} - 0.14$	$V_{H\_x} - 0.11$		V
$V_{GOFFL}$	-	$G_{OFF}$ output low level voltage	$I_{GOFF} = 100\text{ mA}$		84	95	mV
$R_{GON}$	-	Source $R_{DS\_ON}$	$I_{GON} = 100\text{ mA}$		1.11	1.4	$\Omega$
$R_{GOFF}$	-	Sink $R_{DS\_ON}$	$I_{GOFF} = 100\text{ mA}$		0.84	0.95	$\Omega$
<b>Over-temperature protection</b>							
$T_{SD}$	-	Shutdown temperature		170			$^{\circ}\text{C}$
$T_{hys}$	-	Temperature hysteresis			20		$^{\circ}\text{C}$
<b>Standby</b>							
$t_{STBY}$	-	Standby time	See <a href="#">Section 5.6</a>	200	280	350	$\mu\text{s}$
$t_{WUP}$	-	Wake-up time	See <a href="#">Section 5.6</a>	10	20	35	$\mu\text{s}$
$t_{awake}$	-	Wake-up delay	See <a href="#">Section 5.6</a>	90	140	200	$\mu\text{s}$
$t_{stbyfilt}$	-	Standby filter	See <a href="#">Section 5.6</a>	200	280	600	ns

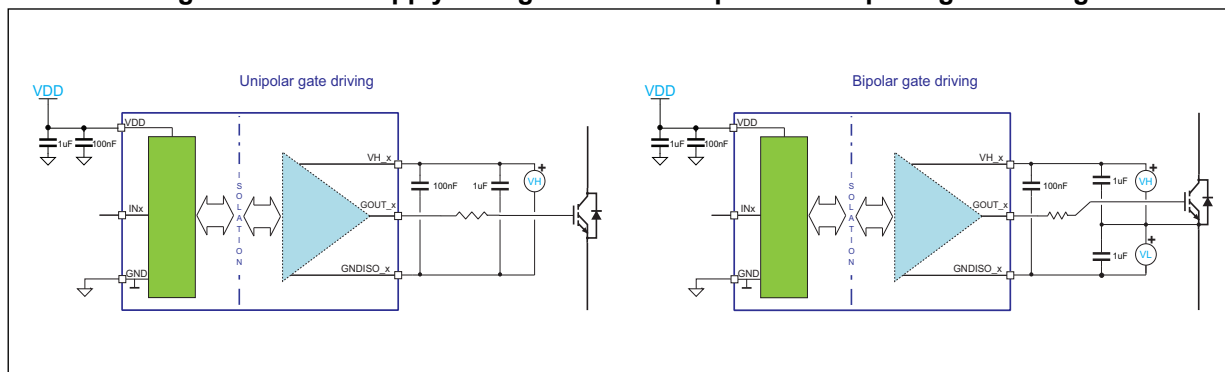
1.  $MT = \max(|t_{Don(A)} - t_{Don(B)}|, |t_{Doff(A)} - t_{Doff(B)}|, |t_{Doff(A)} - t_{Don(B)}|, |t_{Doff(B)} - t_{Don(A)}|)$
2. Characterization data, not tested in production.

## 5 Functional description

### 5.1 Gate driving power supply and UVLO

The STGAP2D is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows to implement either unipolar or bipolar gate driving.

**Figure 3. Power supply configuration for unipolar and bipolar gate driving**



Under-voltage protection is available on the VHX\_x supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VHX\_x voltage goes below the VHoff threshold, the output buffer goes into “safe state”. When VHX\_x voltage reaches the VHon threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VHX\_x supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors, which are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with a value in the range between 1  $\mu$ F and 10  $\mu$ F should be placed close to it.

### 5.2 Power-up, power-down and 'safe state'

The following conditions define the “safe state”:

- GOFF = ON state
- GON = high impedance

Such conditions are maintained at power-up of the isolated side ( $VH\_x < VH_{on}$ ) and during the entire device power-down phase ( $VH < VH_{off}$ ), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on.

If the VHX\_x positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put into safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage side, the device output state depends on the input pins' status.

### 5.3 Control inputs

The device is controlled through the following logic inputs:

- SD: active low shutdown input;
- BRAKE: active low brake input;
- INA, INB: active high logic inputs for channel A and channel B driver outputs.

The operation of the driver IOs is described in [Table 6](#).

**Table 6. Inputs truth table (applicable when device is not in UVLO or "safe state")**

	Input pins <sup>(1)</sup>				Output pins	
	$\overline{\text{SD}}$	$\overline{\text{BRAKE}}$	INA	INB	GOUT_A	GOUT_B
	L	X	X	X	Low	Low
	H	L	X	X	Low	<b>HIGH</b>
	H	H	L	L	Low	Low
	H	H	H	L	<b>HIGH</b>	Low
	H	H	L	H	Low	<b>HIGH</b>
<b>Interlocking</b>	H	H	H	H	Low	Low

1. X: Don't care

A deglitch filter allows input signals with a duration shorter than  $t_{\text{deglitch}}$  to be ignored, thereby preventing noise spikes potentially present in the application from generating unwanted commutations.

### 5.4 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with the LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced into "safe state" until the communication link is properly established again.

### 5.5 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the  $T_{\text{SD}}$  temperature threshold, the device is forced into "safe state". The device operation is restored as soon as the junction temperature is lower than  $T_{\text{SD}} - T_{\text{hys}}$ .

### 5.6 Standby function

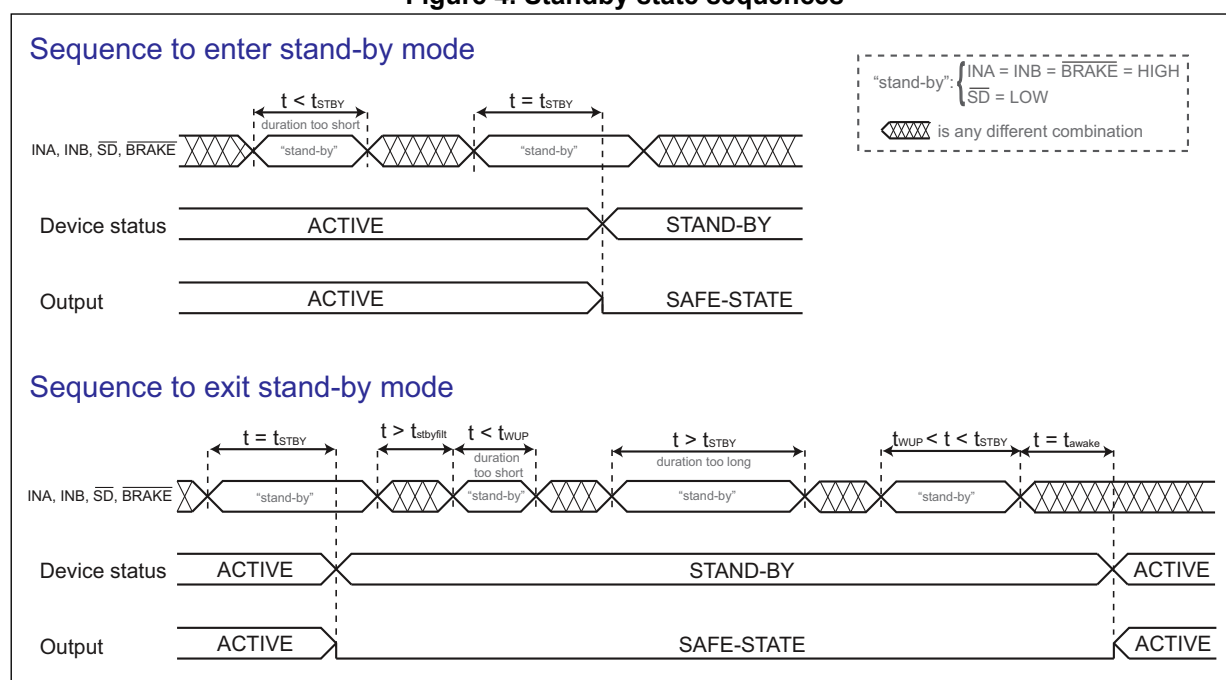
In order to reduce the power consumption of both control interface and gate driving sides the device can be put into standby mode. In standby mode the quiescent current from VDD

and VH\_x supply pins is reduced to I<sub>QDDS</sub> and I<sub>QHS\_x</sub> respectively, and the output remains in 'safe state' (the output is actively forced low).

The way to enter standby is to keep the SD low while keeping the other input pins (INA, INB, and BRAKE) high ("standby" value) for a time longer than  $t_{\text{STBY}}$ . During standby the inputs can change from the "standby" value.

To exit standby, inputs must be put in any combination different from the “standby” value for a time longer than  $t_{\text{stbyfilt}}$ , and then in the “standby” value for a time  $t$  such as  $t_{\text{WUP}} < t < t_{\text{STBY}}$ . When the input configuration is changed from the “standby” value the output is enabled and set according to inputs state. after a time  $t_{\text{awake}}$ .

### Figure 4. Standby state sequences



## 6 Typical application diagram

Figure 5. Typical application diagram - Half-bridge configuration

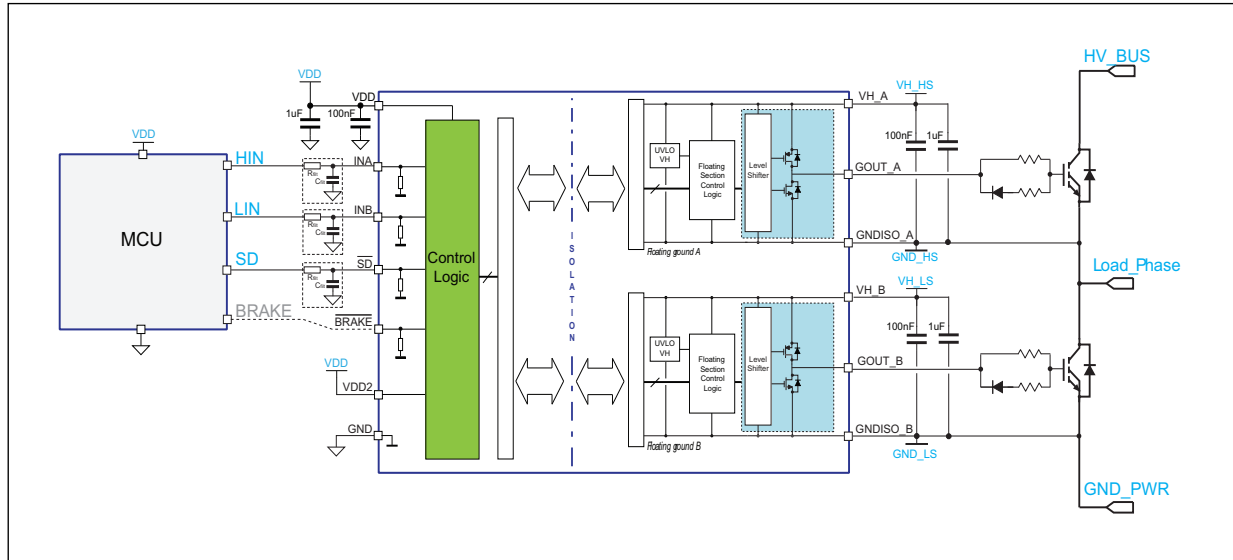
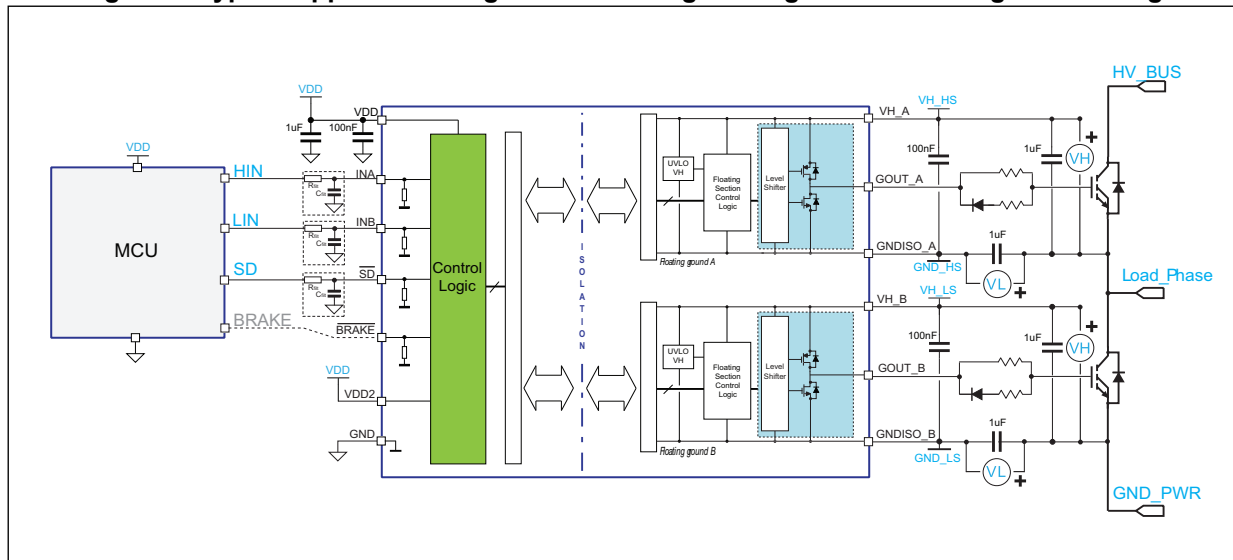


Figure 6. Typical application diagram - Half-bridge configuration with negative driving



## 7 Layout

### 7.1 Layout guidelines and considerations

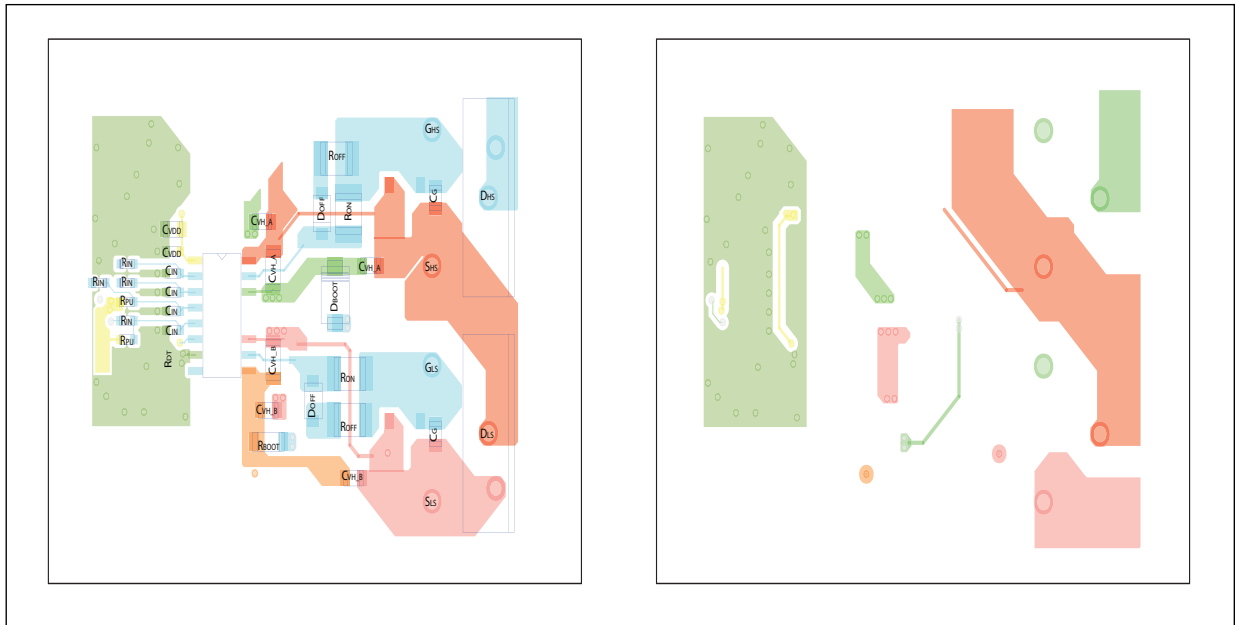
In order to optimize the PCB layout, the following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. A 100 nF capacitor must be placed between VDD and GND and between VH\_x and GNDISO\_x, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current, a second capacitor with a value in the range between 1  $\mu$ F and 10  $\mu$ F should also be placed close to the supply pins.
- As good practice, it is suggested to add filtering capacitors close to logic inputs of the device (INA, INB, BRAKE, SD); in particular for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver, so as to minimize the gate loop area and inductance that might bring noise or ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should be no trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH\_x and GNDISO\_x pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

## 7.2 Layout example

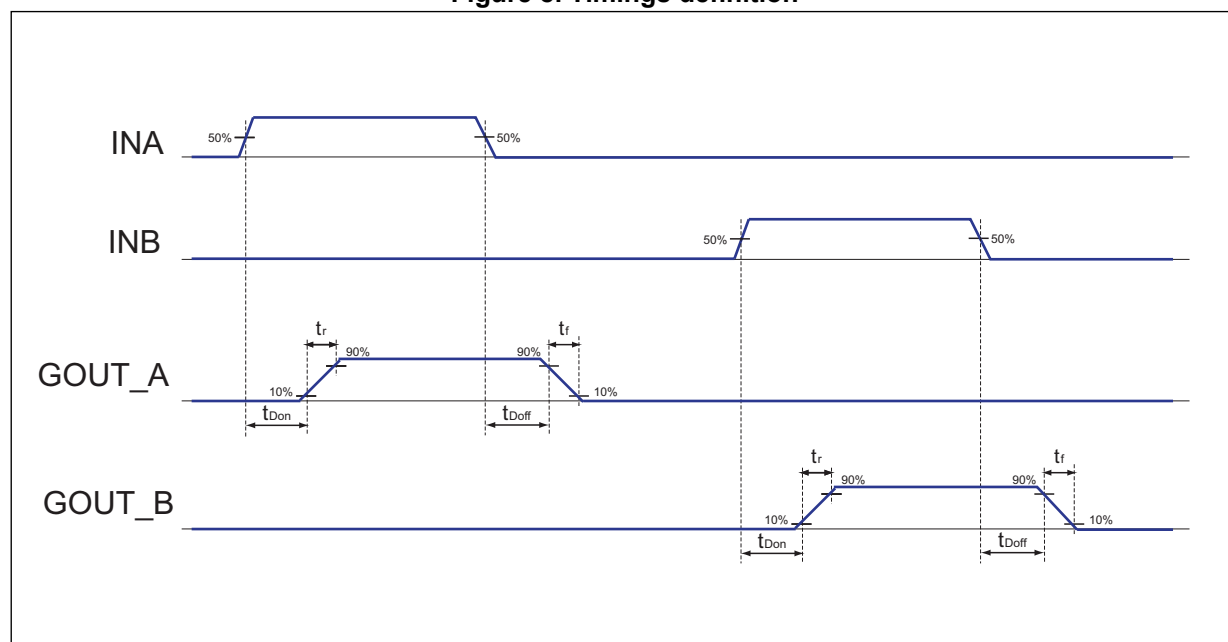
An example of the STGAP2D Half-Bridge PCB layout with main signals highlighted by different colors is shown in [Figure 7](#). It is recommended to follow this example for proper positioning and connection of filtering capacitors.

**Figure 7. Suggested PCB layout for Half-Bridge configuration**

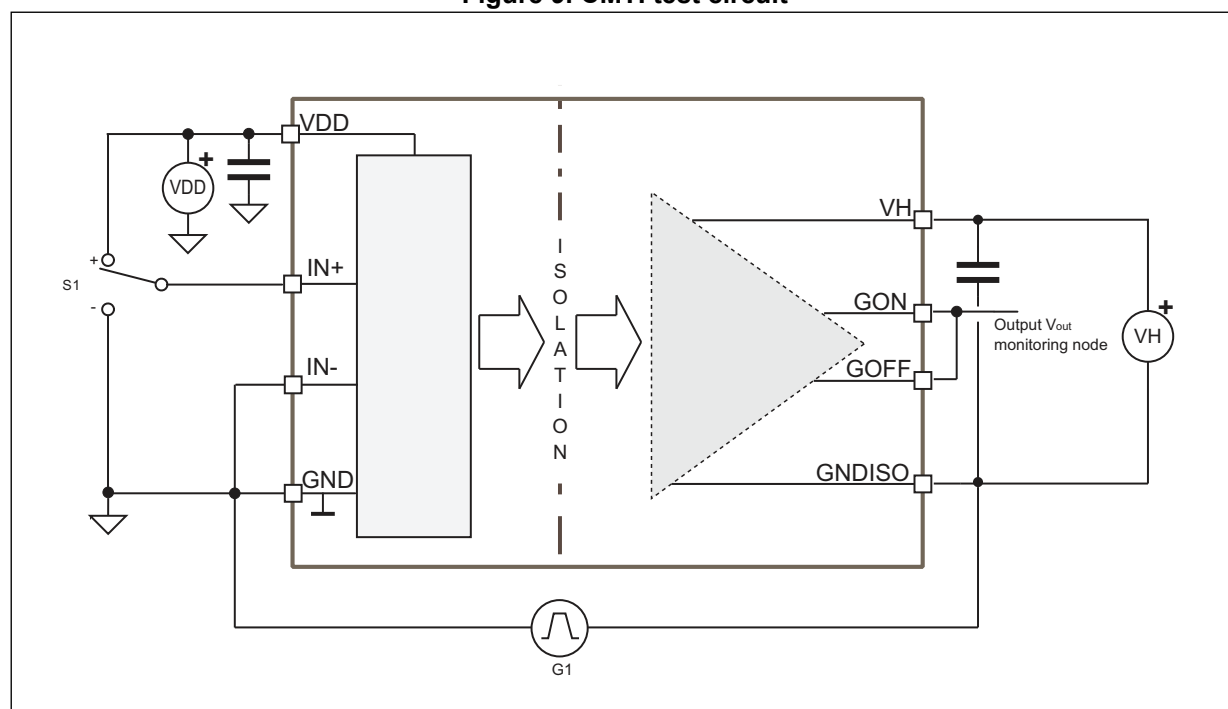


## 8 Testing and characterization information

### Figure 8. Timings definition



**Figure 9. CMTI test circuit**





## 9 Package information

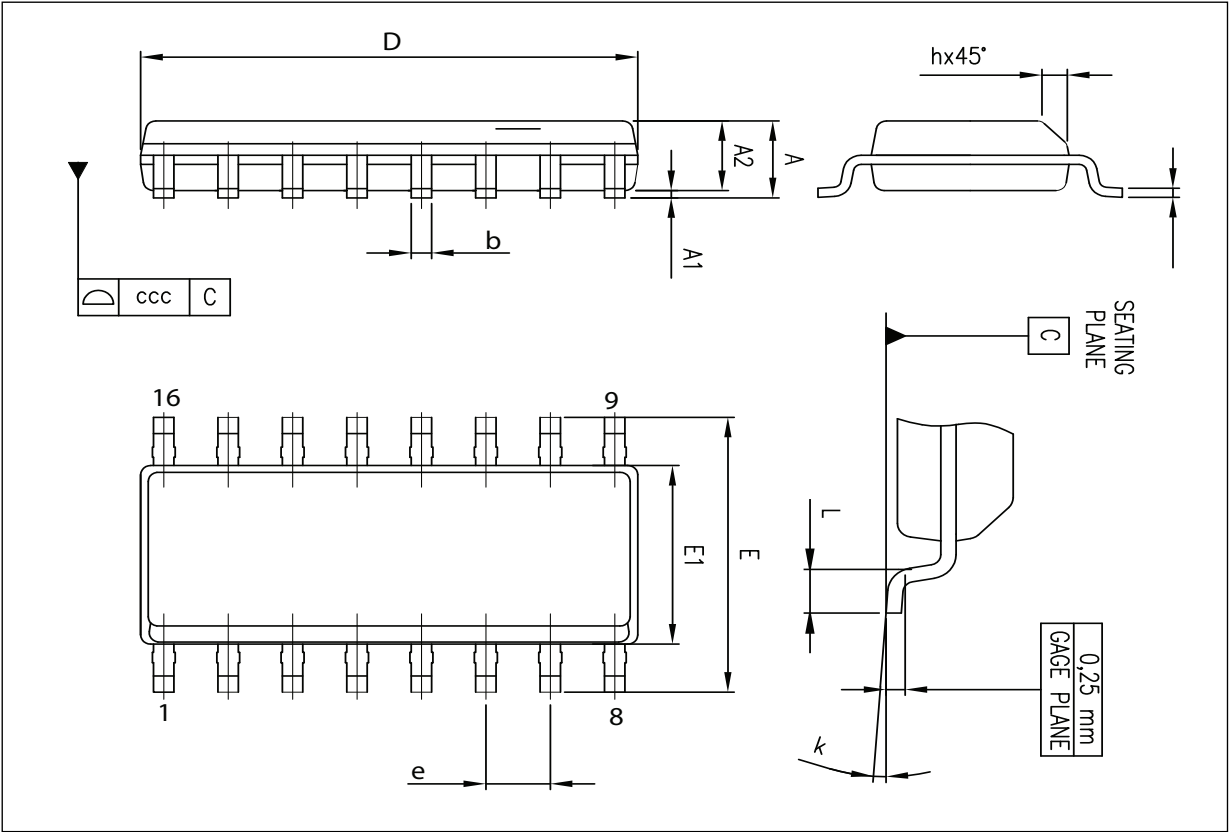
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 7. SO-16 narrow package dimensions**

Dim.	mm			NOTES
	Min.	Typ.	Max.	
A			1.75	
A1	0.10		0.25	
A2	1.25			
B	0.31		0.51	
C	0.17		0.25	
D	9.80	9.90	10.00	(1) (3)
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	(2) (3)
E		1.27		
H	0.25		0.50	
L	0.40		1.27	
K	0		8	DEGREES
Ccc			0.10	

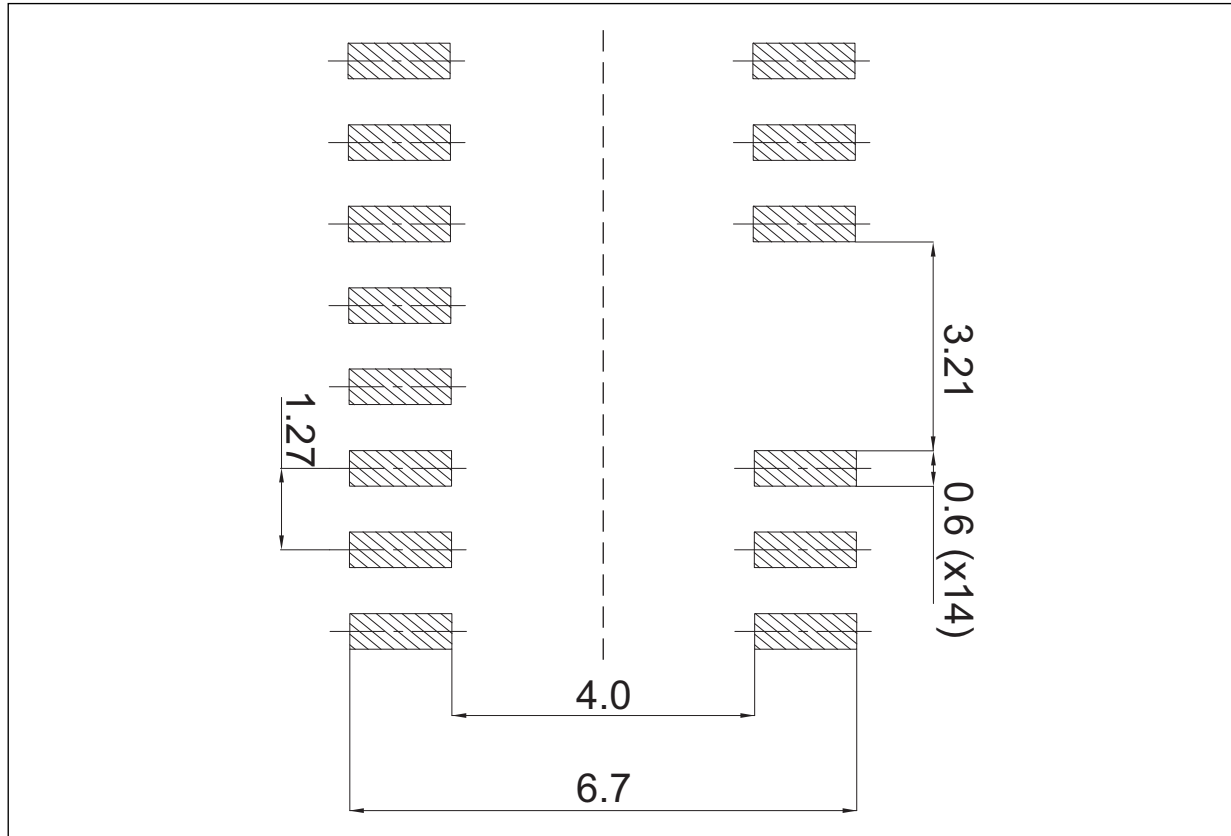
1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.
3. Dimensions referred to the bottom side of the package.

Figure 10. SO-16 narrow package outline



## 10 Suggested land pattern

Figure 11. SO-16 narrow suggested land pattern



## 11 Ordering information

**Table 8. Device summary**

Order code	Output configuration	Package marking	Package	Packaging
STGAP2DM	GOUT	GAP2DM	SO-16	Tube
STGAP2DMTR	GOUT	GAP2DM	SO-16	Tape and reel

## 12 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
24-Aug-2018	1	Initial release.

### IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved