AN4947
Application note

PCB design guidelines for the S2-LP transceiver

Introduction

The S2-LP is a very low power RF transceiver, intended for RF wireless applications in the sub-1 GHz band. It is designed to operate both in the license-free ISM and SRD frequency bands at 433, 868 and 915 MHz.

This application note is intended to accompany the reference designs and provide detailed information regarding the design decisions employed within STMicroelectronics designs. Also, it details the design guidelines for developing a general radio frequency application using an S2-LP device.

The RF performance and the critical maximum peak voltage, spurious and harmonic emission, receiver matching strongly depend on the PCB layout as well as the selection of the matching network components.

For optimal performance, STMicroelectronics recommends the use of the PCB layout design hints described in the following sections. Also, but not less important, STMicroelectronics strongly suggest to use the BOM defined in the reference design, BOM which guarantees, along with a good PCB design, the correct RF performance.

For further information, visit the STMicroelectronics website at *www.st.com*.

Contents

List of tables

List of figures

1 Reference design

Use of the S2-LP transceiver requires only few and low-cost external components. The simplified application circuit for S2-LP (supply decoupling capacitors not included) with SMPS ON is shown in *Figure 1: "SMPS mode ON simplified S2-LP application circuit"*, the one with the SMPS OFF is shown in *Figure 2: "SMPS mode OFF simplified S2-LP application circuit"*. The external components are described in *Table 1: "External component list"*.

Figure 1: SMPS mode ON simplified S2-LP application circuit

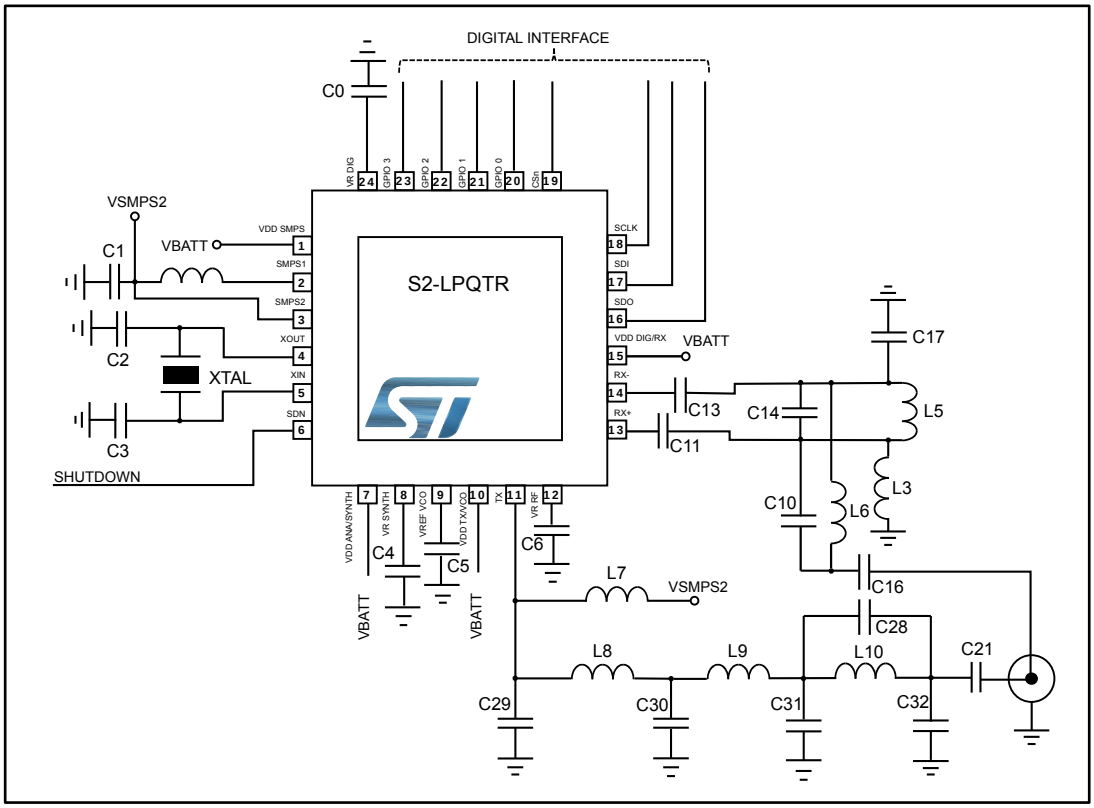


Figure 2: SMPS mode OFF simplified S2-LP application circuit

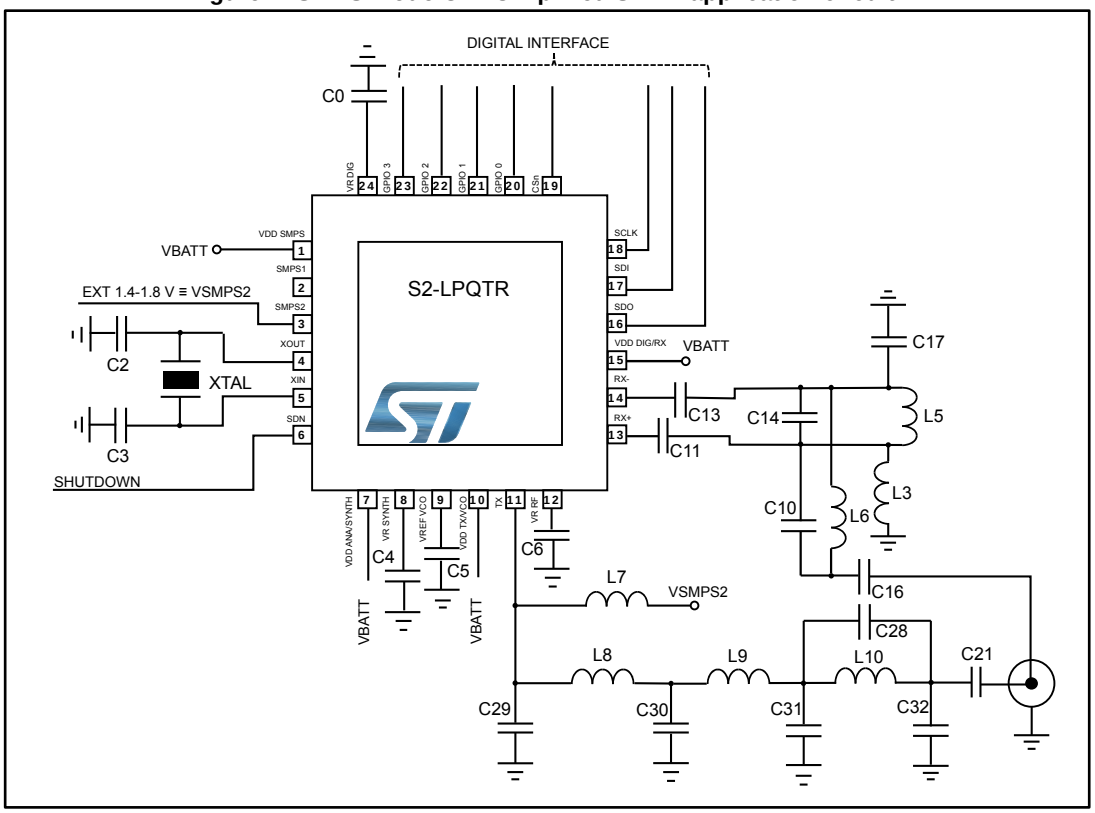


Table 1: External component list

Components	HPM	SMPS OFF	Description
C0	X	X	Decoupling capacitor for on-chip voltage regulator to digital part
C1	X	-	SMPS LC filter capacitors
C2, C3	X	X	Crystal loading capacitors
C4	X	X	Decoupling capacitor for on-chip voltage regulator to synthesizer (LF part)
C5	X	X	Decoupling capacitor for band-gap voltage reference of VCO regulator
C6	X	X	Decoupling capacitor for on-chip voltage regulator to LNA-MIXER
C29, C30, C31, C32	X	X	TX LC filter/matching capacitors
C11, C13, C16, C21	X	X	DC blocking capacitors
C10, C14, C17	X	X	RF balun/matching capacitors
L0	X	-	SMPS LC filter inductor
L7	X	X	RF choke inductor or resonating inductor (upon RF network topology)
L8, L9, L10	X	X	TX LC filter/matching inductors

Components	HPM	SMPS OFF	Description
L3, L5, L6	X	X	RX balun/matching inductors
XTAL	X	X	Crystal

2 RF layout guidelines

2.1 PCB materials

A variety of different materials is used to fabricate PCBs. These materials can also be assembled in a variety of different ways potentially using multiple laminates, different materials and different plated through via structure. A range of finishes can be used making use of materials such as gold, nickel, tin and lead. Typical board materials used for radio circuits are FR4, Rogers R04003 and Roger RT/Duroid. All of these come in a variety of grades and forms and have different electrical characteristics and costs.

The main properties that describe the PCB materials are:

1. Dissipation factor, DF, also known as loss tangent (tanδ), defined as the ratio between the power loss in a dielectric material to the total power transmitted through the dielectric.
2. Dielectric constant, DK, also known as relative permittivity (εr), is a property of a dielectric which determines the electrostatic energy stored per unit volume for unit potential.

Generally, materials are split into “standard loss” and “low loss” categories, with a corresponding cost penalty. Other product considerations such as flammability rating and lead-free assembly narrow these choices. These are beyond the scope of this document.

A summary of the main electrical characteristics of three commonly used board materials for radio products is given in the table below. The cost increases with increased dielectric tolerance and reduced loss.

Table 2: Main board material parameters

Board material	Typical dielectric constant	Dielectric constant tolerance	Typical dissipation factor
FR4	4	+/- 5% -> +/- 25%	0.01
Rogers R04003	3.38	+/- 0.05	0.0027
Rogers RT/Duroid	2.2	+/- 0.03	0.0009

Volume manufacturing requires the least expensive materials to be used while meeting an acceptable level of performance. The PCB plays a leading role in RF performance, so it is necessary to look carefully it. For the type of cost-sensitive applications targeted, a low-cost PCB substrate is mandatory, which means using a standard FR4.

Modern PCB manufacturing achieves very accurate etching and so this is not considered as a performance variable. Z-axis expansion depends on the FR4 material and does not alter much between vendors’ material.

2.2 Two or multi-layer board design

Different choice regarding the number of the layers can be used. A two-layer or an N-layer (where N may be 3 or 4) application board can be used to develop the RF part of an application.

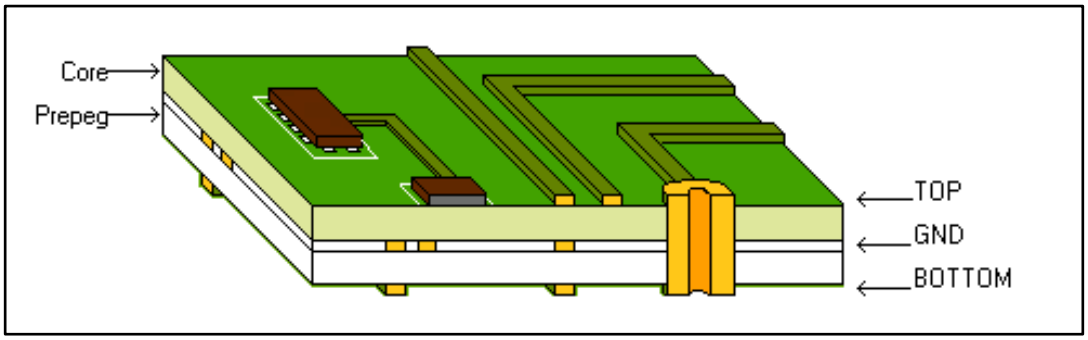
The usual distribution for a 4-layer board should be:

1. TOP layer, used for the RF signals;
2. GROUND layer, used only as ground plane;

3. POWER layer, used DC power lines;
4. BOTTOM layer, used for the low frequency and digital signals.

Placing a distributed ground plane between the RF plane and the power plane enables an evenly distributed RF decoupling layer. In addition, the power plane provides a low impedance trace at radio frequency.

Figure 3: Board layers



The mainly kindness of the multi-layers solution is the possibility to put the ground layer very near to the RF plane to reduce the parasitic effect of the ground plane. All the RF devices need to have a strong ground plane and it is possible to obtain it reducing how much is possible the parasitic effect reducing the distance between the TOP layer and the GROUND layer.

A 2-layer design typically requires a little more care with the PCB routing, but can be successfully implemented for application with a low number of tracks. The power supply trace on the component is made quite thick to present as low as impedance trace as possible. Large areas of ground on this side of the board provide a low impedance path for the decoupling.

A 2-layer PCB is cheaper to manufacture than a 3 or 4-layer PCB. However, to implement microstrip or stripline transmission lines the PCB thickness should not exceed 0.8 mm – 1.00 mm, since the width of the transmission line trace becomes rather large.

2.3 PCB transmission line

Transmission lines maintain chosen impedance, Z_0, from a signal's source to its load, and, unlike all other interconnections, do not resonate however long they are. Transmission lines can easily be made on PCBs by controlling materials and dimension and providing accurate termination resistances at source and/or load. They may also be extended off the PCB with appropriate controlled-impedance cables and connectors.

Comparing the length of a PCB track conductor with the wavelength of the highest frequencies of concern in the relevant medium give us what is called "electrical length" of the track. When a conductor is "electrically long", transmission lines need to be used to maintain the frequency response or to prevent excessive distortion of the wave shape.

Due to the very high frequency of the signal in the RF PCBs, a transmission line technique has to be used. Different type of transmission line structure was studied. The more simple and common used in the RF PCBs is the microstrip trace. Figure 4 illustrates an example of a PCB microstrip, where a trace on the top side of the board is isolated by the PCB dielectric material from the ground plane layer. From knowledge of the physical properties of the PCB it is possible to construct a transmission line trace with the desired characteristic impedance.

A different structure is shown in *Figure 5: "PCB grounded coplanar structure"*. In this case, called grounded coplanar line, the trace is isolated from the ground plane layer by the PCB

dielectric, but also the track is near to the ground plane in the same layer between an air gap.

Many formulas were developed to define the characteristic impedance of the two different structures, but the presentations of these formulas are beyond to this application note.

The grounded coplanar structure guarantees a reduced sensitivity to the PCB thickness variation. This also reduces radiation and coupling effects. Use 50 Ω grounded coplanar lines to connect the SMA connector to the RF matching/filtering network and/or the RF switch wherever possible.

Figure 4: PCB microstrip structure

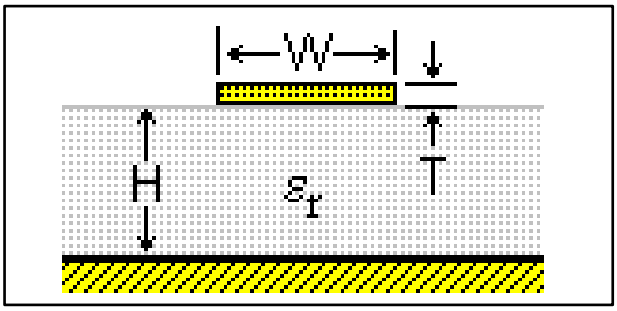
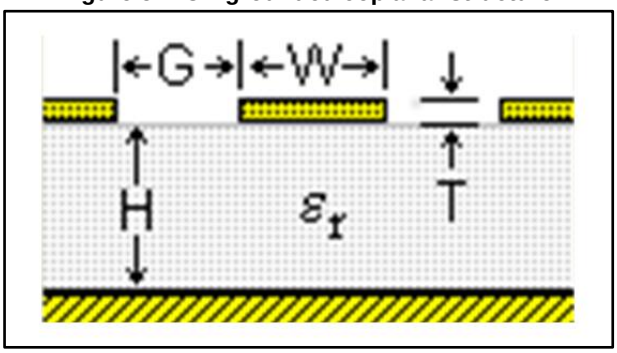


Figure 5: PCB grounded coplanar structure



2.4 Current loops and decoupling

Minimize current loops on PCB layouts by decoupling as close to the port being decoupled to ground as possible. Avoid capacitive coupling by ensuring that each circuit block or port has its own decoupling capacitor. Ensure that each decoupling capacitor has its own via connection to ground. As a rule of thumb, components should not share vias.

The power supplies have to be decoupled as close to the supply pin of the IC as possible to a localized ground pad on the top layer that connected to the main ground plane layer through multiple vias.

By minimizing current loops and through careful and considered decoupling it is possible to avoid noise from the noisy circuit blocks, such as the digital blocks, frequency synthesizer and reference oscillator circuit being coupled to highly sensitive circuit blocks such as LNA and VCO.

2.5 PCB parasitic

An area that is often overlooked during PCB layout is the electrical characteristic of the PCB material itself, components traces and vias. The electrical characteristics of the PCB used to physically mount and connect the circuit components in a high-frequency RF product can have a significant impact on the performance of that product.

The term “PCB parasitic” is used to refer to a physical attribute of the PCB that has an impact on the performance of the circuit. For example, in a high-frequency radio circuit it is simple to see how a long thin track will be inductive and a large pad over a ground plan will be capacitive.

In addition, the impedance of the connections between circuit components and the ground plane must also be modeled in the real circuits. The vias used to connect the different layers will have an associated parasitic parallel capacitance and inductance, which will form a parallel resonant circuit. Typically for a 1.6 mm thickness PCB material, a single via can add 1.2 nH of inductance and 0.5 pF of capacitance, depending upon the via dimensions and PCB dielectric material, although the effects can be minimized by ensuring that the inter-via spacing is of λ/30.

3 Passive components

Passive components play a fundamental role in the success of a winning PCB. Following is a brief description of the physical properties of the capacitors and inductors components that can help with the circuit design and the choice of the components.

ST strongly recommends using only the values and types of items specified in the BOM of the S2-LP application board, since a change in their value and/or type can create a different behavior of the RF characteristic of the application.

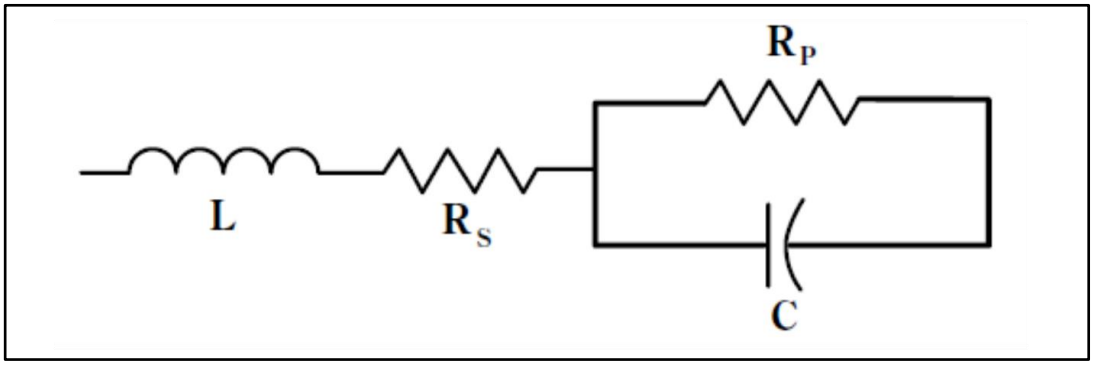
3.1 Capacitors

A capacitor is a passive electrical component used to store energy in an electrical field. The forms of practical capacitors vary widely, but all contain at least two electrical conductors separated by a dielectric.

Capacitors differ from each other for construction techniques and materials used to manufacture. A lot of different types of capacitors exist (double-layer, polyester, polypropylene and so on), but this document will focus on the surface mount versions of ceramics only. The other types of capacitors are not indicated for characteristic or cost for the application targeted in this document.

A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic of the equivalent circuit is shown in *Figure 6: "Capacitor equivalent circuit"*.

Figure 6: Capacitor equivalent circuit



Typically for the capacitors are defined the ESR (equivalent series resistance) and the ESL (equivalent series inductance). The term ESR combines all losses both series and parallel in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection. Same discourse for the ESL that is the equivalent series inductor comprised of three components: pad layout, capacitor height and power plane spreading inductance.

The main differences between ceramic dielectric types are the temperature coefficient of capacitance and the dielectric loss. COG and NP0 (negative-positive-zero, i.e ±0) dielectrics have the lowest losses and are used in filtering, matching and so on.

For RF applications it is generally recommended that multilayer (or monolithic) ceramic capacitors with a COG dielectric material, which is a highly stable class I dielectric offering a linear temperature coefficient, low loss and stable electrical properties over time, voltage and frequency.

For RF decoupling purposes select a capacitor value such that for the frequency to be decoupled is close to or just above the series resonant frequency (SRF) of the capacitor. At SRF the parasitic impedance resonates with the device capacitance to form a series tuned circuit and the impedance presented by the capacitor is the effective series resistance (ESR).

For DC blocking or coupling applications at RF, typically a capacitor with low insertion loss and a good quality factor is required. Since a capacitor's quality factor is inversely proportional to its ESR, select a capacitor with a low ESR and ensure that the SRF of the capacitor is greater than the frequency of operation. If the working frequency is above the SRF of the capacitor, it will appear inductive.

3.2 Inductors

An inductor is a passive electrical component used to store energy in its magnetic field. Any conductor has inductance. An inductor is typically made of a wire or other conductor wound into a coil, to increase the magnetic field.

Inductors differ from each other for construction techniques and materials used to manufacture. A lot of different types of inductors exist (air core inductor, ferromagnetic core inductor and variable inductor), but this document will focus on the inductors useful for RF only. Usually in RF the air core inductors are used. The term air core describes an inductor that does not use a magnetic core made of ferromagnetic material, but coil wound on plastic, ceramic, or other nonmagnetic form. They are lower inductance than ferromagnetic core coils, but are used at high frequencies because they are free from energy losses called core losses.

Usually the real circuit of an inductor is composed of a series resistance and a parallel capacitor. The parallel capacitor is considered to be the inter-winding capacitance that exists the turns of the inductor. If the inductor is placed over a ground plane then this capacitance will also include the capacitance that exists between the inductor and the ground plane. The series resistor can be considered as the resistance of the inductor winding.

In term of circuit performance, as already mentioned for the capacitors, the self-resonant frequency, and the quality factor are the main inductor parameters, especially for the circuit where the losses need to be minimized. At the self-resonant frequency, the inductor impedance is at maximum. For frequency above the self-resonance the inductor behavior change and it will appear capacitive.

In general wirewound inductors have a higher quality factor than a multilayer equivalent. They will also reflect and radiate more energy which can give rise to higher emission levels, especially in term of self-coupling. Inductive coupling can give rise to undesired circuit operation: to minimize coupling mount the inductors in sensitive circuit areas at 90 degrees to one another.

4 Design recommendation when using S2-LP RF IC

The S2-LP device uses a class-E type TX matching network with a typical output power level of +14 dBm. Two basic types of board layout configurations exist at all the frequency bands: the split TX/RX type and the direct tie type. In the split TX/RX type the TX and RX paths are separated and connected by an antenna switch. In the direct tie type the RX and TX paths are connected directly without any additional RF switch. In this application note, the case with the direct tie type is explored.

The schematic of the S2-LP direct tie type and SMPS on application board is shown in *Figure 7: "S2-LP direct tie and SMPS on application board schematic"*. The layout of the critical zone of the S2-LP is shown in *Figure 8: "S2-LP direct tie type application board layout"*.

Figure 7: S2-LP direct tie and SMPS on application board schematic

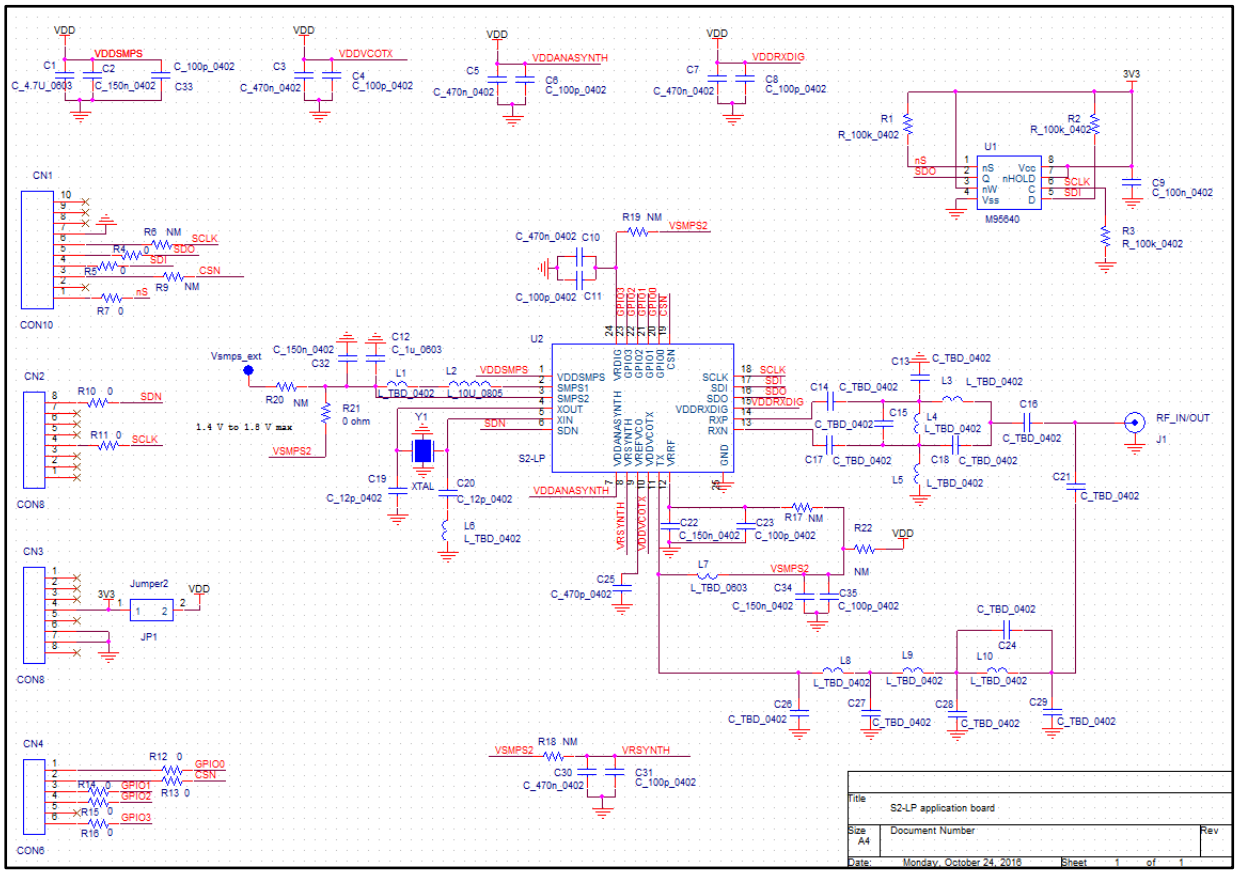
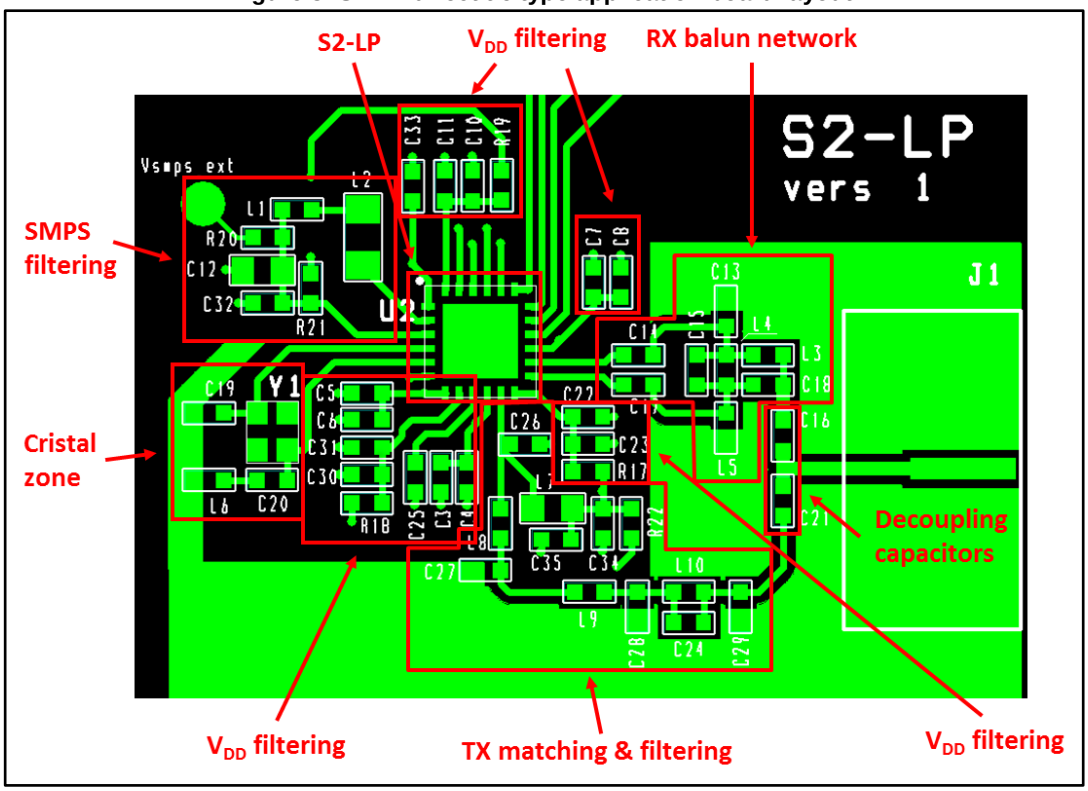


Figure 8: S2-LP direct tie type application board layout



Here is the key guidance on how to realize the layout of the S2-LP application board.

- The discrete balun of the RX path has to be placed as close to the RX pins as possible.
- The traces that connect the two RX pins to the balun network (differential traces) should be of equal length. If the two differential signals are un-balanced, common-mode problems can be generated.
- Route differential traces closely together. Differential receivers are designed to be sensitive to the difference between a pair of inputs, but also to be insensitive to a common-mode shift of those input. Therefore, if any external noise is coupled equally into the differential traces, the receiver will be insensitive to this (common mode coupled) noise. More closely differential traces are routed together, more equal will any coupled noise be on each trace, therefore better will be the rejection of the noise in the circuit.
- The parallel inductors in the RX path (and in general) should be mutually perpendicular to avoid mutual couplings. If no perpendicular position is possible, turn away their interposing capacitors or resistors.
- The TX and RX section should be separated by a ground plane in the top layer to reduce the coupling.
- Connect the TX and RX section using 50 Ω grounded coplanar lines wherever possible. This type of line structure reduces radiation and coupling effects. Also the characteristic impedance of the track is less sensible to the PCB thickness variation.
- The interconnections between the elements are not considered transmission lines because their lengths are much shorter than the wavelength and, thus, their impedance is not critical. As results, their recommended width is smallest possible. In this way, the parasitic capacitances to ground can be minimized.
- The choke inductor (L7) has to be placed as close to the TX pin of the RF IC as possible.

- Inductors have to be put perpendicular to each other to improve filter attenuation at higher harmonic frequencies. If it is not possible to put the inductances in perpendicular, do not place the inductors in parallel to each other.
- Put the L1 and L2 inductors in the perpendicular mode to avoid coupling.
- Don’t put a ground plane near to the SMPS to reduce the coupling with the traces of the SMPS.
- The smaller VDD bypass capacitor should be kept as close to the VDD pin as possible.
- The exposed pad of the S2-LP IC should be connected to the ground layer below with the maximum number of via possible. The exposed pad should also be connected to the top layer ground metal to further improve RF grounding using also diagonal trace connections where is possible.
- The crystal should be placed as close as possible to the S2-LP IC. The crystal capacitors should also be placed near to the crystal pads. This to ensure that wire parasitic capacitances are kept as low as possible to reduce the frequency offsets that may occur. Use to stabilize the crystal frequency only COG capacitor due their poor value variation affected by the temperature variation.
- Add large and continuous ground metallization on the top layer. To provide a good RF ground, the RF voltage potentials should be equal along the entire ground area because this helps maintain good VDD filtering.
- Three or four layers board is strongly recommended. Put the ground layer very close to the top layer to obtain a good ground plane reference. A thickness between top layer and ground layer of 0.3 mm is suggested.
- If it is not possible to use three or four layers board, it is necessary to fill the area under the RF part of the board (RF IC, TX matching and filtering network, RX balun and SMPS section) with ground metal to reduce or eliminate radiation emissions. Board routing and wiring should not be placed in this region to prevent coupling effects and to ensure a good ground reference plane to the RF parts.
- Connect all the ground metallization and/or layers with as many vias as possible. It is also recommended that the ground return path between the ground vias of the TX and RX networks and the ground vias of the S2-LP IC should not be blocked in any way: the return current should see a clear unhindered pathway through the ground plane to the back of the S2-LP IC.

5 Reference

[1] S2-LP datasheet.

6 Revision history

Table 3: Document revision history

Date	Version	Changes
08-Nov-2016	1	Initial release.
20-Feb-2017	2	Updated *Section 2.2: "Two or multi-layer board design"*.

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